# Datasheet

## APM32F103x4x6x8xB

## Arm® Cortex®-M3 based 32-bit MCU

**Version: V 1.3**

# 1. Features

- System Architecture
  - 32-bit Arm® Cortex®-M3 core
  - Up to 96MHz working frequency
- Clock and Memories
  - HSECLK: 4MHz~16MHz external crystal oscillator supported
  - LSECLK: 32.768KHz RTC oscillator supported
  - HSICLK: 8 MHz RC oscillator with calibration
  - LSICLK: 40 KHz RC oscillator
  - Flash : maximum 128 Kbytes
  - SRAM : maximum 20 Kbytes
- Power supply and low-power mode
  - 2.0 ~ 3.6 V reset supply voltage
  - Support programmable voltage Detector(PVD)
  - Sleep, Stop and Standby modes
  - $V_{Bat}$ power supply can support RTC and backup registers
- FPU
  - Independent FPU module supports floating point operations
- ADCs and Temperature Sensor
  - 2 12-bit ADCs, 16 input channels are supported
  - ADC voltage conversion range: 0~$V_{DDA}$
  - Double-sample and hold capability supported
  - 1 on-chip temperature sensor
- I/O
  - 80/51/37/26 I/Os selectable, depending on models and packages
  - All I/O pins are mappable to 16 external interrupt
- DMA
  - 1 DMA, 7 separate configurable channels are supported
- Timers
  - 1 16-bit advanced control timer TMR1, support dead zone control and emergency braking functions
  - 3 16-bit general-purpose timers TMR2/3/4, each with up to 4 independent channels to support input capture, output comparison, PWM, pulse count and other functions
  - 2 watchdog timers(Independent IWDT and Window WWDT)
  - 1 24-bit autodecrement SysTick Timer
- Communication Interfaces
  - 3 USARTs, support ISO7816, LIN and IrDA
  - 2 I2C, support SMBus/PMBus
  - 2 SPIs with a maximum transfer speed of 18Mbps
  - 1 QSPI, support single - and four-wire access to Flash
  - 1 USB 2.0 FS Device
  - 1 CAN 2.0B, USBD and CAN can work independently at the same time)
- 1 CRC Unit
- 96-bit UID
- Serial wire debug SWD and JTAG interfaces
- Chip Packaging
  - LQFP100/LQFP64/LQFP48/QFN36
- Applications
  - Medical devices, PC peripherals, industrial control, smart meters, household appliances

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# 2. Overview

The APM32F103xB series chips are Arm® Cortex®-M3 core based 32-bit microcontrollers with a maximum operating frequency of 96MHz. Built-in AHB high-performance bus, combined with high-speed memory and DMA for fast data processing and storage. The built-in APB advanced peripheral bus expands the rich peripherals and enhanced I/O, ensuring fast connection and control flexibility. The chips are equipped with a powerful FPU floating-point arithmetic processing unit that supports single-precision data processing instructions and data types.

Built-in up to 128K bytes of flash memory and 20K bytes of SRAM memory, and all models include 2 12-bit ADCs, 3 general-purpose 16-bit timers, 1 advanced control timer and 1 temperature sensor, as well as standard communication interfaces: 2 I2C interfaces, 2 SPI interfaces, 1 QSPI interface, 3 USART interfaces, 1 USB 2.0 FS interface and 1 CAN 2.0B interface(USBD and CAN can work independently at the same time).

Operating voltage is 2.0V ~ 3.6V, there are two types of operating temperature range selectable: -40°C~+85°C and -40°C~+105°C. Available for four different package forms of LQFP100/LQFP64/LQFP48/QFN36, with different peripherals and I/O configurations.

For information about the Arm® Cortex®-M3 core, please refer to the Arm®Cortex®-M3 technical reference manual, which can be downloaded from ARM’s website.

# 3. Features Description

See the following table for specific APM32F030x6/x8 product functions and peripheral configuration.

Table 1. Functions and peripherals of APM32F103xB

| Product | | APM32F103xB | | | |
|---|---|---|---|---|---|
| | | TB | CB | RB | VB |
| Packaging | | QFN36 | LQFP48 | LQFP 64 | LQFP 100 |
| Flash(Kbytes) | | 128 | | | |
| SRAM(Kbytes) | | 20 | | | |
| Timers | General-purpose(16-bit) | 3 | | | |
| | Advanced(16-bit) | 1 | | | |
| | SysTick | 1 | | | |
| | Watchdog | 2 | | | |
| | RTC | 1 | | | |
| Communication Interfaces | SPI | 1 | 2 | | |
| | QSPI | 1 | | | |
| | I2C | 1 | 2 | | |
| | USART | 2 | 3 | | |
| | CAN2.0B | 1 | | | |
| | USB2.0 FS | 1 | | | |
| 12 bit ADC | Unit | 2 | | | |
| | Channel | 10 | | 16 | |
| GPIOs | | 26 | 37 | 51 | 80 |
| CPU@Max. frequency | | M3@96MHz | | | |
| FPU | | 1 | | | |
| Operating voltage | | 2.0 V~ 3.6 V | | | |

## 3.1. Arm® Cortex®-M3 Core

APM32F103xB series with built-in Arm® Cortex®-M3 core, 96MHz working frequency, and are compatible with ARM's tools and softwares.

System diagram of APM32F103xB series products is shown in Figure 5.

## 3.2. Memory

Table 2. Memory Description

| Memory | The biggest byte | Function |
|---|---|---|
| Embedded High-speed Flash | 128 Kbytes | For storing programs and data |
| Embedded Static Memory | 20 Kbytes | Can be accessed in bytes, halfwords(16 bits) or full words(32 bits) |

## 3.3. Power Management

### 3.3.1. Power Supply Schemes

Table 3. Power Supply Schemes

| Name | Voltage Range | Description |
|---|---|---|
| $V_{DD}$ | 2.0 ~ 3.6V | $V_{DD}$ directly supplies power to IO port, and $V_{DD}$ supplies power to core circuit through voltage regulator. |
| $V_{DDA}$ | 2.4 ~ 3.6V | Connected to $V_{DD}$, it supplies power to the analog parts of ADC, reset module, RC oscillator and PLL. When ADC is being used, $V_{DDA}$ is greater than or equal to 2.4V. $V_{DDA}$ and $V_{SSA}$ must be connected to $V_{DD}$ and $V_{SS}$ respectively. |
| $V_{BAT}$ | 1.8V ~ 3.6V | Automatically supply power to RTC, external 32KHz oscillator and backup registers when $V_{DD}$ is off. |

Note: See Figure 8 for more details on how to connect power supply pins.

### 3.3.2. Voltage Regulator

There are three main modes of voltage regulator. The working mode of MCU can be adjusted by voltage regulator to reduce power consumption.

Table 4. Operation Modes of Voltage Regulator

| Name | Description |
|---|---|
| Main Mode(MR) | 1.6V power supply(core, memory, peripherals) in normal regulation mode |
| Low Power Mode(LPR) | 1.6V power supply in low power mode to preserve the contents of register and SRAM |
| Power Down Mode | Used in Standby mode: the regulator output is in high |

| Name | Description |
|---|---|
| | impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost) |

This regulator is always enabled after reset, and outputs with high impedance in power-down mode.

### 3.3.3. Power Supply Monitor

Two circuits of power-on reset (POR) and power-down reset (PDR), are integrated inside the product. When $V_{DD}$ reaches the set threshold $V_{POR/PDR}$, the system works normally. When $V_{DD}$ is below the specified threshold $V_{POR/PDR}$, the system remains in a reset state without the need for an external reset circuit.

For details of $V_{POR/PDR}$, please refer to the electrical feature in chapter 5.

### 3.3.4. Low Power Mode

The product supports the following three low power consumption modes, which can be configured by users to meet the best application requirements.

Table 5. **Low Power Consumption Mode**

| Mode Types | Description |
|---|---|
| Sleep Mode | In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs. |
| Stop Mode | The Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. At this point, part of the 1.6V power supply are stopped, resulting in the HSECLK, HSICLK, and PLL clocks are disabled. The voltage regulator is either in normal or in low-power mode. Interrupt, event wakeup configured as EINT can wake up the CPU from stop mode. |
| Standby Mode | The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that part of 1.6 V domain is powered off. The HSECLK, HSICLK, and PLL clocks are also switched off. The contents of SRAM and registers are lost, but contents of the backup registers will still remain, and the standby circuit will still work. The external reset signal on NRST, IWDT, will reset an ascending edge on the WKUP pin or the RTC clock will then terminate the chip standby mode. |

Note: The RTC, the IWDT, and the corresponding clock sources are not stopped by

entering stop or standby mode. QSPI interrupts cannot wake up low power mode.

## 3.4. Clocks and Startup

The internal 8MHz RC oscillator serves as the default clock for system startup, and can be switched to the external 4-16mhz clock with failure monitoring through configuration.

When an external clock failure is detected, the system will automatically switch to an internal RC oscillator, and if an interrupt is set, the software can receive the related interrupt.

The frequencies of AHB high-speed APB(APB2) and low-speed APB(APB1) can be configured through the predivider. The maximum frequency of AHB and high-speed APB is 96MHz and that of low speed APB is 48MHz.

See Figure 6 for details on the clock tree.

## 3.5. RTC and Backup Registers

The RTC has a set of continuously running counters, which can provide calendar alarm interruption and stage interruption functions with softwares. Its clock source can choose external 32.768khz crystal oscillator, internal 40KHz low-speed RC oscillator or external high-speed clock with 128 frequency division. Moreover, the RTC clock can be calibrated for errors through a 512Hz signal.

A backup register for 10 16-bit registers to hold 20 bytes of user data when VDD is off.

RTC and backup registers are powered by $V_{DD}$ when $V_{DD}$ is in effect; otherwise, it will be powered by $V_{BAT}$ pins. System or power reset source reset, waking up from standby mode, does not cause the reset of RTC and backup register.

## 3.6. Boot Modes

At startup, you can choose one of three bootstrap modes through the bootstrap pin:

- Boot from User Flash
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1.

## 3.7. CRC (Cyclic Redundancy Check) Calculation Unit

The CRC (Cyclic Redundancy Check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

The CRC calculation unit helps compute a signature of the software during runTime, to be compared with a reference signature generated at link-Time and stored at a given memory location.

## 3.8. General Purpose IO Port

80/51/37/26 I/O is available for the product, and the specific selection can refer to the model and package. All I/O can be mapped to 16 external interrupt controllers, and most of I/O support 5V logic level input.

### 3.8.1. General-purpose urpose Input\Output Interface

The product can be up to 80 GPIO pins, each of the GPIOs can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers. I/Os on APB2 with up to 18 MHz toggling speed.

## 3.9. Interrupt Controller

### 3.9.1. Nested Vectored Interrupt Controller (NVIC)

- It can handle 16 priority levels and maskable interrupt channels simultaneously. The closely coupled NVIC gives low-latency interrupt processing.
- Interrupt entry vector table address passed directly to the core
- Allow early processing of interrupts.
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state is automatically saved.
- Interrupt entry restored on interrupt exit with no instruction overhead
- This hardware block provides flexible interrupt management features with minimal interrupt latency.

### 3.9.2. External Interrupt/Event Controller (EINT)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. Up to 80 GPIOs can be connected to the 16 external interrupt lines. The EINT can detect an external line with a pulse width shorter than the Internal APB2 clock period.

## 3.10. Floating Point Unit (FPU)

The product has a embedded independent FPU floating-point arithmetic processing unit that

supports the IEEE754 standard and supports single-precision floating-point operations.

## 3.11. DMA

The flexible 7-channel general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I2C, USART, general-purpose and advanced-control Timers TMRx and ADC.

## 3.12. Timer

The product includes an advanced-control Timer (TMR1), three general-purpose Timers (TMR2/3/4), an independent watchdog Timer, a window watchdog Timer, and a SysTickTimer.

The following table compares the features of the advanced-control and general-purpose Timers:

Table 6. Timer Feature Comparison

| Type of Timer | SysTick Timer | General-purpose Timer | | | Advanced -control Timer |
|---|---|---|---|---|---|
| Timer | Sys Tick Timer | TMR2 | TMR3 | TRM4 | TMR1 |
| Counter Resolution | 24-bit | 16-bit | | | 16-bit |
| Counter Type | Down | Up, down, up/down | | | Up, down, up/down |
| Prescaler Factor | - | Any integer between 1 and 65536 | | | Any integer between 1 and 65536 |
| DMA Request generation | - | Yes | | | Yes |
| Capture/Compare Channels | - | 4 | | | 4 |
| Complementary Outputs | - | No | | | Yes |
| Function Specification | Dedicated for OS<br>Automatic reload function<br>Maskable system interrupt generation when the counter reaches 0<br>Programmable clock | Synchronization or event chaining function provided.<br>Counters can be frozen in debug mode<br>Can be used to generate PWM outputs | | | Complementary PWM outputs with programmable inserted dead-Times<br>If configured as a general-purpose 16-bit Timer, it has the same features as the TMRx Timer. |

| | | | |
|---|---|---|---|
| | source | Each Timer has independent DMA request generation.<br>It can handle quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors | If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).<br>In debug mode, the advanced-control Timer counter can be frozen and the PWM outputs disabled.<br>Synchronization or event chaining provided |

## 3.13. Watchdog（WDT）

The product includes two watchdogs, providing greater security, Time accuracy and flexibility. The two watchdogs(independent and window watchdog)can be used for detecting and resolving failures caused by software errors. When the counter reaches a given Timeout value, an interrupt is triggered (for window watchdogs only) or a system reset is generated.

Table 7. Watchdog

| Watchdog | Counter Resolution | Counter Type | Prescale Factor | functional |
|---|---|---|---|---|
| Independent Watchdog | 12-bit | down | Any integer between 1 and 256 | It is clocked from an independent 40 kHz internal RC oscillator and as it operates independently from the main clock, it can operate in stop and standby modes.<br>Reset the device when a problem occurs.<br>As a free-running Timer for application Timeout management.<br>It is hardware- or software-configurable through the option bytes.<br>The counter can be frozen in debug mode. |
| Window Watchdog | 7-bit | down | - | It can be set as free-running.<br>Reset the device when a problem occurs.<br>It is clocked from the main clock. It has an early warning interrupt capability.<br>The counter can be frozen in debug mode. |

## 3.14. Peripheral Interface

### 3.14.1. I²C Bus

Two embedded I²C (I²C1, I²C2) bus interfaces can operate in multimaster or slave mode. They can support standard and fast modes. They support dual slave addressing (7-bit only) and both

7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded. They can be served by DMA and they support SM Bus 2.0/PM Bus.

$I^2C$3/4 bus extended the function of $I^2C$ 1/2. They can operate in standard, fast and high speed mode. The fast mode and high speed mode devices are backwards compatible.

### 3.14.2. Universal Synchronous/Asynchronous Receiver Transmitter (USART)

Three USART communication interfaces are embedded, providing hardware management of the CTS and RTS signals, and IrDA SIR ENDEC supported. They are ISO 7816 compliant and have LIN Master/Slave capability. One of the USART interfaces is able to communicate at speeds of up to 4.5 Mbit/s. The other available interfaces communicate at up to 2.25 Mbit/s. All USART interfaces can be served by the DMA controller.

### 3.14.3. Serial Peripheral Interface (SPI)

Two SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes while the frame is configurable to 8 bits or 16 bits. Both SPIs can be served by the DMA controller.

### 3.14.4. Quad SPI Controller (QSPI)

The product has an embedded QSPI dedicated communication interface that can be connected to external flash via single, dual or quad SPI mode, supporting 8-bit, 16-bit and 32-bit access. There are 8 bytes of transmit FIFO and 8 bytes of receive FIFO.

### 3.14.5. Controller Area Network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

### 3.14.6. Universe Serial Bus (USBD)

The product embeds a USBD device peripheral compatible with the USB2.0 full-speed 12 Mbs. The USBD interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSECLK crystal oscillator).

### 3.14.7. Simultaneous Use of USBD Interface and CAN Interface:

When USBD and CAN are used together, you need to:

- Write 0x00000001 at the base address offset 0x100 of the USBD.

- The PA11 and PA12 pins are for USBD and CAN is used to multiplex other pins.

### 3.14.8. ADC (Analog/Digital Converter)

Two 12-bit analog-to-digital converters are embedded into APM32F103x8xb performance line devices and each ADC shares up to 16 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single shunt

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose Timers (TMRx) and the advanced-control Timer (TMR1) can be internally connected to the ADC start trigger, injection trigger, and DMA trigger respectively, to allow the application to synchronize A/D conversion and Timers.

### 3.14.9. Temperature Sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2 V < VDDA < 3.6 V. The temperature sensor is internally connected to the ADC12_IN16 input channel which is used to convert the sensor output voltage into a digital value.

### 3.14.10. Debug Interface (SWJ-DP)

The product supports serial debug interface (SW-DP) and JTAG (JTAG-DP) debug interface.

The JTAG interface provides a 5-pin standard JTAG interface for the AHB access port. The SW-DP interface provides a 2-pin (data + clock) interface to the AHB module.

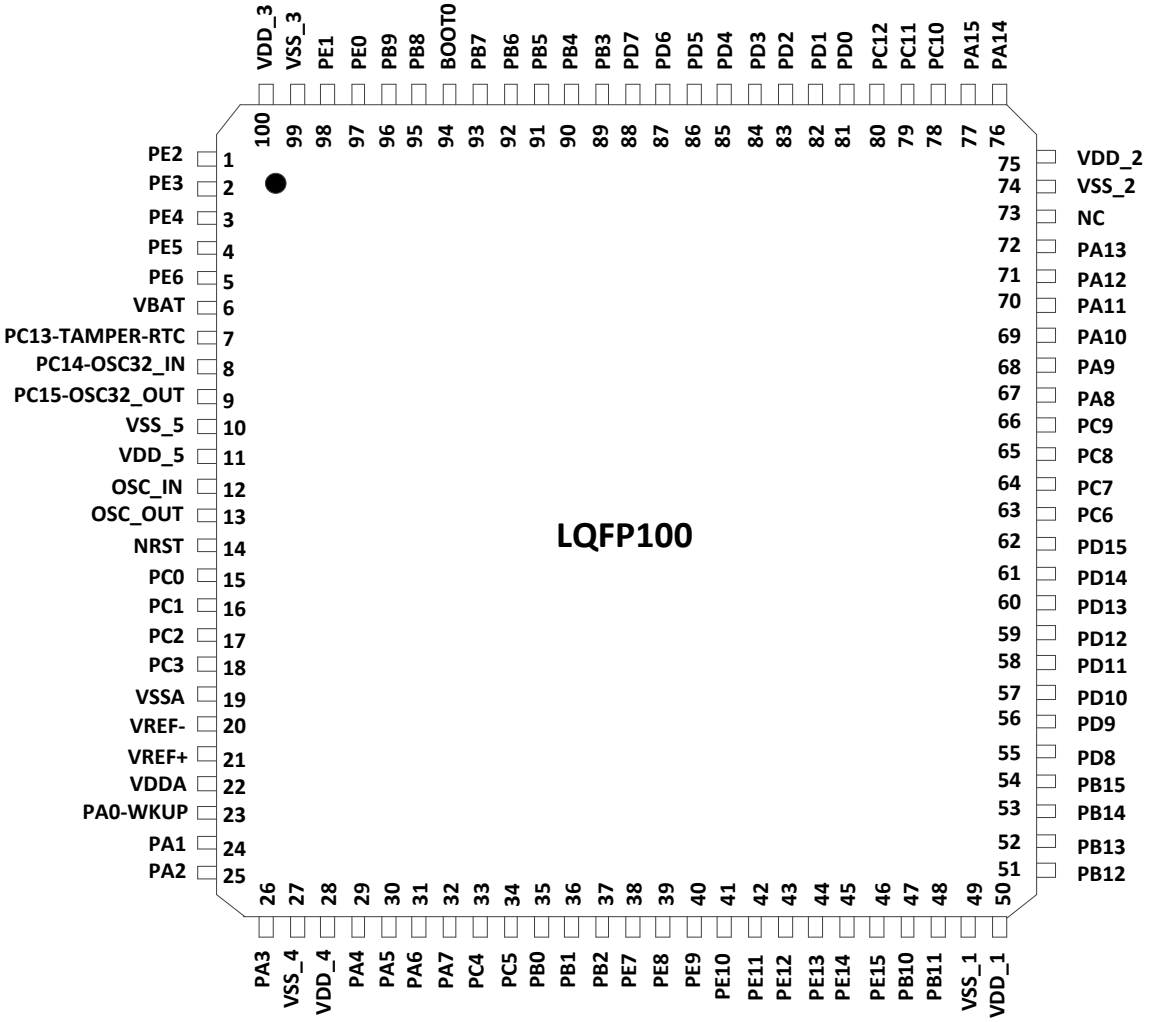
The two pins of the SW-DP interface and the five pins of the JTAG interface are multiplexed.

# 4. Pin Features

## 4.1. Pinouts and Pin Description

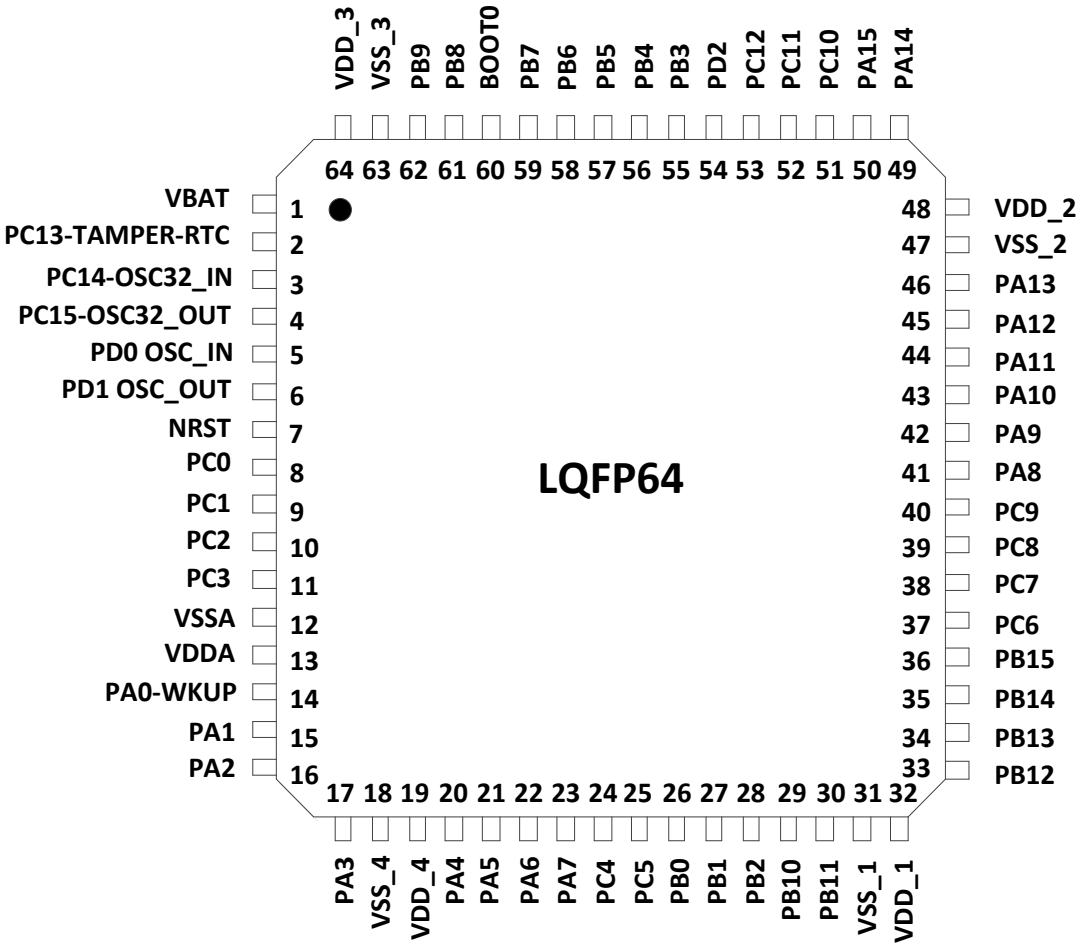
### 4.1.1. APM32F103xB Series LQFP100

Figure 1. LQFP100 Pinout



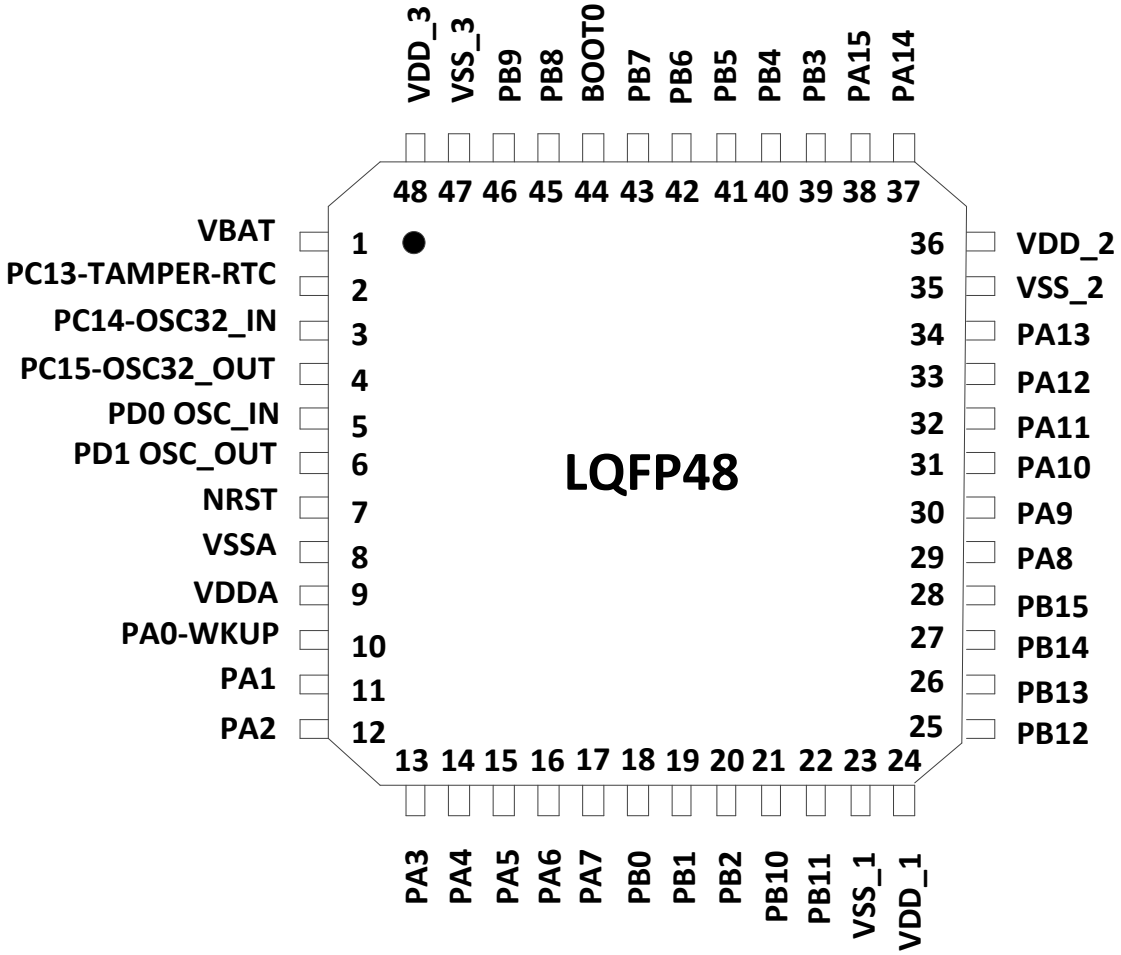
### 4.1.2. APM32F103xB Series LQFP64

Figure 2. LQFP64 Pinout



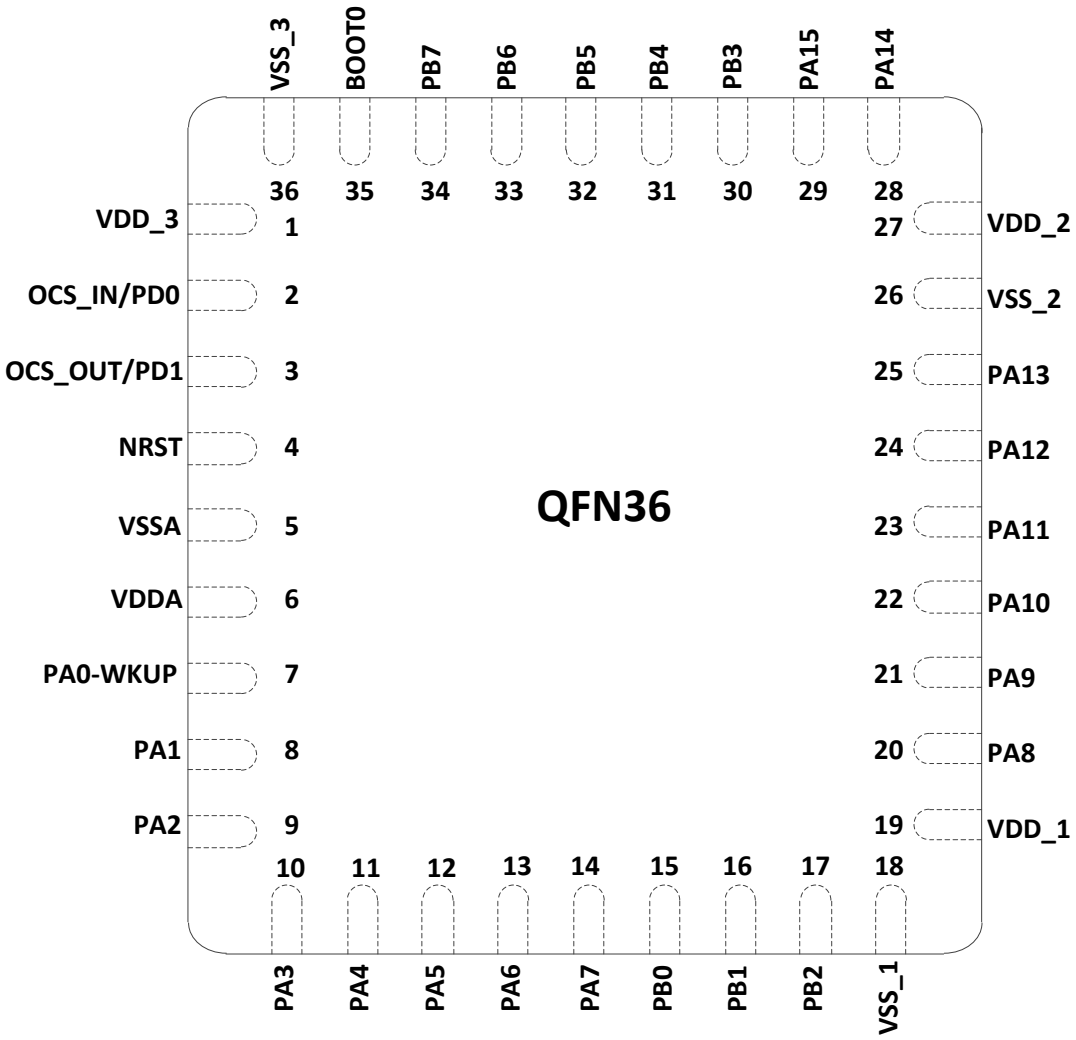
### 4.1.3. APM32F103xB Series LQFP48

Figure 3. LQFP48 Pinout



### 4.1.4. APM32F103xB Series QFN36

Figure 4. QFN36 Pinout



## 4.2. Pin Description

Table 8. APM32F103xB Pin Definitions

| Pin Name | Pins | | | | Type (1) | I/O level (2) | Main Function (3) | Alternate functions | |
|---|---|---|---|---|---|---|---|---|---|
| | LQFP48 | LQFP64 | LQFP100 | QFN36 | | | (after reset) | Default | Remap |
| PE2 | - | - | 1 | - | I/O | FT | PE2 | TRACECK | - |
| PE3 | - | - | 2 | - | I/O | FT | PE3 | TRACED0 | - |
| PE4 | - | - | 3 | - | I/O | FT | PE4 | TRACED1 | - |
| PE5 | - | - | 4 | - | I/O | FT | PE5 | TRACED2 | - |
| PE6 | - | - | 5 | - | I/O | FT | PE6 | TRACED3 | - |
| $V_{BAT}$ | 1 | 1 | 6 | - | S | - | $V_{BAT}$ | - | - |
| PC13-TAMPER-RTC(4) | 2 | 2 | 7 | - | I/O | - | PC13(5) | TAMPER-RTC | - |
| PC14-OSC32_IN(4) | 3 | 3 | 8 | - | I/O | - | PC14(5) | OSC32_IN | - |
| PC15-OSC32_OUT(4) | 4 | 4 | 9 | - | I/O | - | PC15(5) | OSC32_OUT | - |
| $V_{SS}$_5 | - | - | 10 | - | S | - | $V_{SS}$_5 | - | - |
| $V_{DD}$_5 | - | - | 11 | - | S | - | $V_{DD}$_5 | - | - |
| OSC_IN | 5 | 5 | 12 | 2 | I | - | OSC_IN | - | PD0(7) |
| OSC_OUT | 6 | 6 | 13 | 3 | O | - | OSC_OUT | - | PD1(7) |
| NRST | 7 | 7 | 14 | 4 | I/O | - | NRST | - | - |
| PC0 | - | 8 | 15 | - | I/O | - | PC0 | ADC12_IN10 | - |
| PC1 | - | 9 | 16 | - | I/O | - | PC1 | ADC12_IN11 | - |
| PC2 | - | 10 | 17 | - | I/O | - | PC2 | ADC12_IN12 | - |
| PC3 | - | 11 | 18 | - | I/O | - | PC3 | ADC12_IN13 | - |
| $V_{SSA}$ | 8 | 12 | 19 | 5 | S | - | $V_{SSA}$ | - | - |
| $V_{REF-}$ | - | - | 20 | - | S | - | $V_{REF-}$ | - | - |
| $V_{REF+}$ | - | - | 21 | - | S | - | $V_{REF+}$ | - | - |
| $V_{DDA}$ | 9 | 13 | 22 | 6 | S | - | $V_{DDA}$ | - | - |

| Pin Name | Pins | | | | Type (1) | I/O level (2) | Main Function (3) | Alternate functions | |
|---|---|---|---|---|---|---|---|---|---|
| | LQFP48 | LQFP64 | LQFP100 | QFN36 | | | (after reset) | Default | Remap |
| PA0-WKUP | 10 | 14 | 23 | 7 | I/O | - | PA0 | WKUP/ USART2_CTS(6) / ADC12_IN0/ TMR2_CH1_ETR(6) | - |
| PA1 | 11 | 15 | 24 | 8 | I/O | - | PA1 | USART2_RTS(6)/ ADC12_IN1/ TMR2_CH2(6) | - |
| PA2 | 12 | 16 | 25 | 9 | I/O | - | PA2 | USART2_TX(6)/ ADC12_IN2/ TMR2_CH3(6) | - |
| PA3 | 13 | 17 | 26 | 10 | I/O | - | PA3 | USART2_RX(6)/ ADC12_IN3/ TMR2_CH4(6) | - |
| $V_{SS}$_4 | - | 18 | 27 | - | S | - | $V_{SS}$_4 | - | - |
| $V_{DD}$_4 | - | 19 | 28 | - | S | - | $V_{DD}$_4 | - | - |
| PA4 | 14 | 20 | 29 | 11 | I/O | - | PA4 | SPI1_NSS(6)/ USART2_CK(6) / ADC12_IN4 | - |
| PA5 | 15 | 21 | 30 | 12 | I/O | - | PA5 | SPI1_SCK(6)/ ADC12_IN5 | - |
| PA6 | 16 | 22 | 31 | 13 | I/O | | PA6 | SPI1_MISO(6)/ ADC12_IN6/ TMR3_CH1(6) | TMR1_BKIN |
| PA7 | 17 | 23 | 32 | 14 | I/O | | PA7 | SPI1_MOSI(6)/ ADC12_IN7/ TMR3_CH2(6) | TMR1_CH1N |
| PC4 | - | 24 | 33 | - | I/O | - | PC4 | ADC12_IN14 | - |
| PC5 | - | 25 | 34 | - | I/O | - | PC5 | ADC12_IN15 | - |
| PB0 | 18 | 26 | 35 | 15 | I/O | - | PB0 | ADC12_IN8/ TMR3_CH3(6) | TMR1_CH2N |
| PB1 | 19 | 27 | 36 | 16 | I/O | - | PB1 | ADC12_IN9/ TMR3_CH4(6) | TMR1_CH3N |

| Pin Name | Pins | | | | Type (1) | I/O level (2) | Main Function (3) | Alternate functions | |
|---|---|---|---|---|---|---|---|---|---|
| | LQFP48 | LQFP64 | LQFP100 | QFN36 | | | (after reset) | Default | Remap |
| PB2 | 20 | 28 | 37 | 17 | I/O | FT | PB2/BOOT1 | - | - |
| PE7 | - | - | 38 | - | I/O | FT | PE7 | - | TMR1_ETR |
| PE8 | - | - | 39 | - | I/O | FT | PE8 | - | TMR1_CH1N |
| PE9 | - | - | 40 | - | I/O | FT | PE9 | - | TMR1_CH1 |
| PE10 | - | - | 41 | - | I/O | FT | PE10 | - | TMR1_CH2N |
| PE11 | - | - | 42 | - | I/O | FT | PE11 | - | TMR1_CH2 |
| PE12 | - | - | 43 | - | I/O | FT | PE12 | - | TMR1_CH3N |
| PE13 | - | - | 44 | - | I/O | FT | PE13 | - | TMR1_CH3 |
| PE14 | - | - | 45 | - | I/O | FT | PE14 | - | TMR1_CH4 |
| PE15 | - | - | 46 | - | I/O | FT | PE15 | - | TMR1_BKIN |
| PB10 | 21 | 29 | 47 | - | I/O | FT | PB10 | $I^2C2\_SCL$/ $I^2C4\_SCL$/ USART3_TX(6) | TMR2_CH3 |
| PB11 | 22 | 30 | 48 | - | I/O | FT | PB11 | $I^2C2\_SDA$/ $I^2C4\_SDA$/ USART3_RX(6) | TMR2_CH4 |
| $V_{SS}$_1 | 23 | 31 | 49 | 18 | S | - | $V_{SS}$_1 | - | - |
| $V_{DD}$_1 | 24 | 32 | 50 | 19 | S | - | $V_{DD}$_1 | - | - |
| PB12 | 25 | 33 | 51 | - | I/O | FT | PB12 | SPI2_NSS/ $I^2C2\_SMBAI$/ USART3_CK(6)/ TMR1_BKIN(6) | |
| PB13 | 26 | 34 | 52 | - | I/O | FT | PB13 | SPI2_SCK/ USART3_CTS(6)/ TMR1_CH1N(6)/ QSPI_IO0 | |
| PB14 | 27 | 35 | 53 | - | I/O | FT | PB14 | SPI2_MISO/ USART3_RTS(6) / TMR1_CH2N(6)/ | |

| Pin Name | Pins | | | | Type (1) | I/O level (2) | Main Function (3) | Alternate functions | |
|---|---|---|---|---|---|---|---|---|---|
| | LQFP48 | LQFP64 | LQFP100 | QFN36 | | | (after reset) | Default | Remap |
| | | | | | | | | QSPI_IO1 | |
| PB15 | 28 | 36 | 54 | - | I/O | FT | PB15 | SPI2_MOSI/ TMR1_CH3N(6)/ QSPI_IO2 | - |
| PD8 | - | - | 55 | - | I/O | FT | PD8 | QSPI_IO3 | USART3_TX |
| PD9 | - | - | 56 | - | I/O | FT | PD9 | - | USART3_RX |
| PD10 | - | - | 57 | - | I/O | FT | PD10 | QSPI_CMU | USART3_CK |
| PD11 | - | - | 58 | - | I/O | FT | PD11 | - | USART3_CTS |
| PD12 | - | - | 59 | - | I/O | FT | PD12 | QSPI_SS_N | TMR4_CH1/ USART3_RTS |
| PD13 | - | - | 60 | - | I/O | FT | PD13 | - | TMR4_CH2 |
| PD14 | - | - | 61 | - | I/O | FT | PD14 | - | TMR4_CH3 |
| PD15 | - | - | 62 | - | I/O | FT | PD15 | - | TMR4_CH4 |
| PC6 | - | 37 | 63 | - | I/O | FT | PC6 | - | TMR3_CH1 |
| PC7 | - | 38 | 64 | - | I/O | FT | PC7 | - | TMR3_CH2 |
| PC8 | - | 39 | 65 | - | I/O | FT | PC8 | - | TMR3_CH3 |
| PC9 | - | 40 | 66 | - | I/O | FT | PC9 | - | TMR3_CH4 |
| PA8 | 29 | 41 | 67 | 20 | I/O | FT | PA8 | USART1_CK/ TMR1_CH1(6)/ MCO | - |
| PA9 | 30 | 42 | 68 | 21 | I/O | FT | PA9 | USART1_TX(6) / TMR1_CH2(6) | - |
| PA10 | 31 | 43 | 69 | 22 | I/O | FT | PA10 | USART1_RX(6)/ TMR1_CH3(6) | - |
| PA11 | 32 | 44 | 70 | 23 | I/O | FT | PA11 | USART1_CTS/USBDM / USB2DM/ CAN_RX(6)/ TMR1_CH4(6) | - |
| PA12 | 33 | 45 | 71 | 24 | I/O | FT | PA12 | USART1_RTS/ | - |

| Pin Name | Pins | | | | Type (1) | I/O level (2) | Main Function (3) | Alternate functions | |
|---|---|---|---|---|---|---|---|---|---|
| | LQFP48 | LQFP64 | LQFP100 | QFN36 | | | (after reset) | Default | Remap |
| | | | | | | | | USBDP/USB2DP/ CAN_TX(6)/ TMR1_ETR(6) | |
| PA13 | 34 | 46 | 72 | 25 | I/O | FT | JTMS/ SWDIO | - | PA13 |
| Disconnected | - | - | 73 | - | - | - | - | Disconnected | - |
| $V_{SS}$_2 | 35 | 47 | 74 | 26 | S | | $V_{SS}$_2 | - | - |
| $V_{DD}$_2 | 36 | 48 | 75 | 27 | S | | $V_{DD}$_2 | - | - |
| PA14 | 37 | 49 | 76 | 28 | I/O | FT | JTCK/ SWCLK | - | PA14 |
| PA15 | 38 | 50 | 77 | 29 | I/O | FT | JTDI | - | TMR2_CH1_ETR/PA15/ SPI1_NSS |
| PC10 | - | 51 | 78 | - | I/O | FT | PC10 | - | USART3_TX |
| PC11 | - | 52 | 79 | - | I/O | FT | PC11 | - | USART3_RX |
| PC12 | - | 53 | 80 | - | I/O | FT | PC12 | - | USART3_CK |
| PD0 | - | - | 81 | 2 | I/O | FT | PD0 | - | CAN_RX |
| PD1 | - | - | 82 | 3 | I/O | FT | PD1 | - | CAN_TX |
| PD2 | - | 54 | 83 | - | I/O | FT | PD2 | TMR3_ETR | - |
| PD3 | - | - | 84 | - | I/O | FT | PD3 | - | USART2_CTS |
| PD4 | - | - | 85 | - | I/O | FT | PD4 | - | USART2_RTS |
| PD5 | - | - | 86 | - | I/O | FT | PD5 | - | USART2_TX |
| PD6 | - | - | 87 | - | I/O | FT | PD6 | - | USART2_RX |
| PD7 | - | - | 88 | - | I/O | FT | PD7 | - | USART2_CK |
| PB3 | 39 | 55 | 89 | 30 | I/O | FT | JTDO | - | PB3/ TRACESWO TMR2_CH2/ SPI1_SCK |

| Pin Name | Pins | | | | Type (1) | I/O level (2) | Main Function (3) | Alternate functions | |
|---|---|---|---|---|---|---|---|---|---|
| | LQFP48 | LQFP64 | LQFP100 | QFN36 | | | (after reset) | Default | Remap |
| PB4 | 40 | 56 | 90 | 31 | I/O | FT | NJTRST | - | PB4/ TMR3_CH1/ SPI1_MISO |
| PB5 | 41 | 57 | 91 | 32 | I/O | - | PB5 | I²C1_SMBAI | TMR3_CH2/ SPI1_MOSI |
| PB6 | 42 | 58 | 92 | 33 | I/O | FT | PB6 | I²C1_SCL(6) /I²C3_SCL/ TMR4_CH1(6) | USART1_TX |
| PB7 | 43 | 59 | 93 | 34 | I/O | FT | PB7 | I²C1_SDA(6) /I²C3_SDA/ TMR4_CH2(6) | USART1_RX |
| BOOT0 | 44 | 60 | 94 | 35 | I | - | BOOT0 | - | - |
| PB8 | 45 | 61 | 95 | - | I/O | FT | PB8 | TMR4_CH3(6) | I²C1_SCL/ ( I²C3_SCL/ CAN_RX |
| PB9 | 46 | 62 | 96 | - | I/O | FT | PB9 | TMR4_CH4(6) | I²C1_SDA ( I²C3_SDA ) / CAN_TX |
| PE0 | - | - | 97 | - | I/O | FT | PE0 | TMR4_ETR | - |
| PE1 | - | - | 98 | - | I/O | FT | PE1 | - | - |
| $V_{SS}$_3 | 47 | 63 | 99 | 36 | S | - | $V_{SS}$_3 | - | - |
| $V_{DD}$_3 | 48 | 64 | 100 | 1 | S | - | $V_{DD}$_3 | - | - |

(1) I = input, O = output, S = supply, HiZ = high resistance

(2) FT = 5V tolerant.

(3) Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripheral that is included. For example, if a device has only one SPI and two USARTs, they will be called SPI1 and USART1 & USART2, respectively.

(4) PC13, PC14 and PC15 are supplied through the power switch since the switch only sinks a limited amount of current (3mA). The use of GPIOs from PC13 to PC15 in output mode is

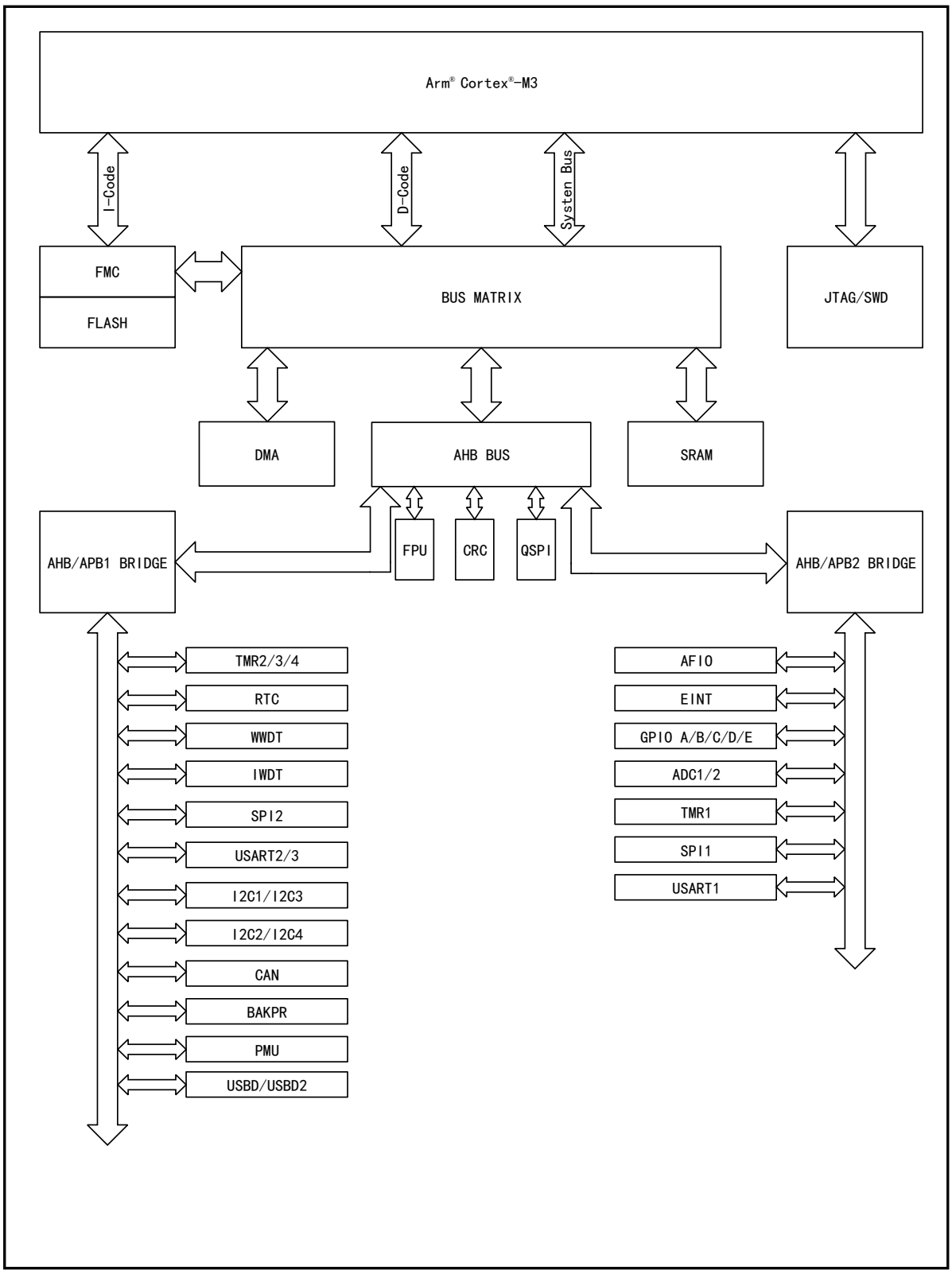
limited: only one GPIO can be used at a Time, the speed should not exceed 2 MHz with a maximum load of 30pF and these IOs must not be used as a current source (e.g. to drive an LED).

(5) Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BAKR register description sections in the reference manual.

(6) This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the alternate function I/O and debug configuration section in the reference manual.

## 4.3. System Diagram

Figure 5. APM32F103xB Series System Diagram

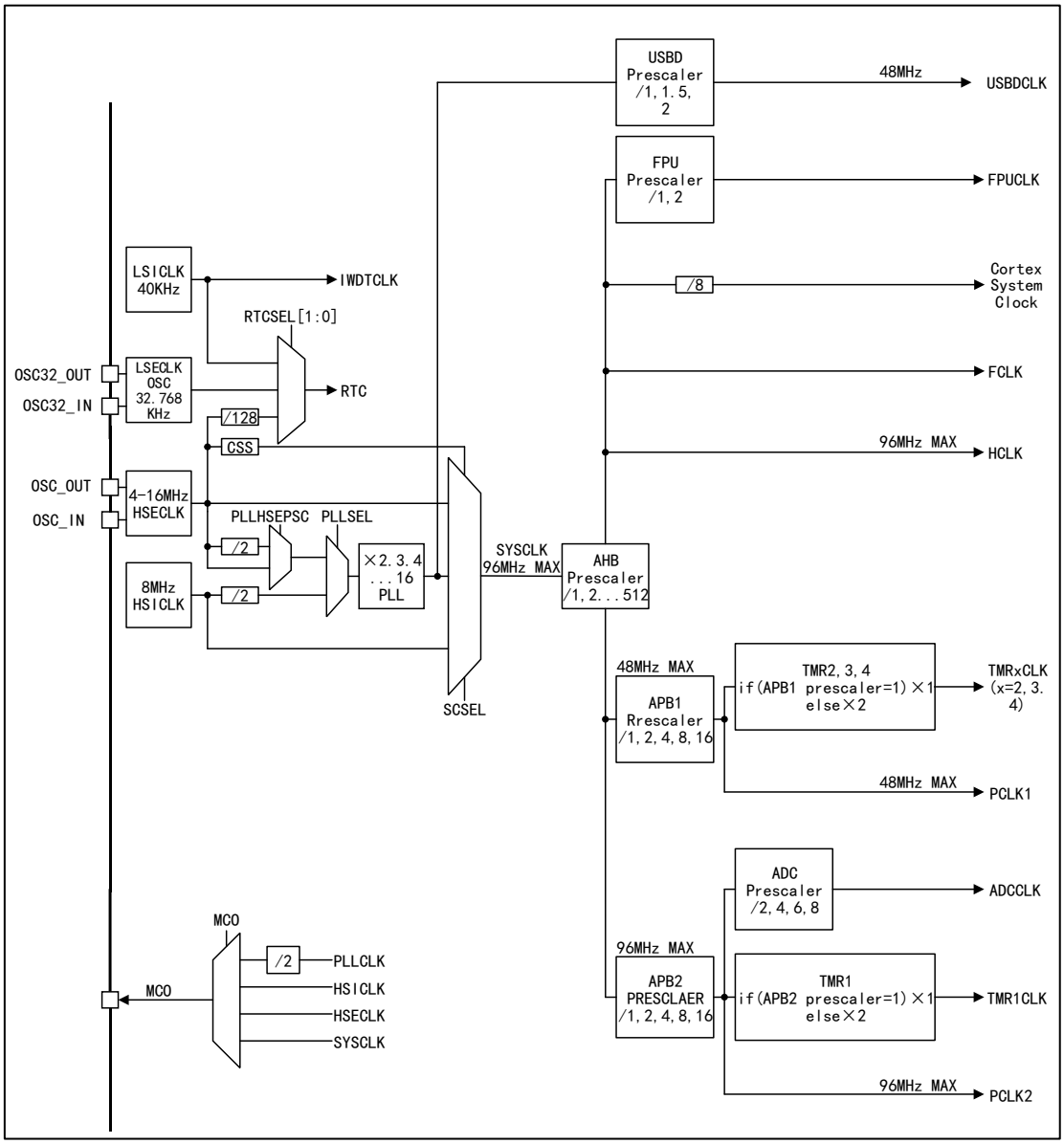



(1) The max frequency for APM32F103xB series AHB and high-speed APB is 96MHz;

(2) The max frequency for APM32F103xB series low-speed APB clock is 48MHz.

## 4.4. Clock Tree

Figure 6. APM32F103xB Series Clock Tree

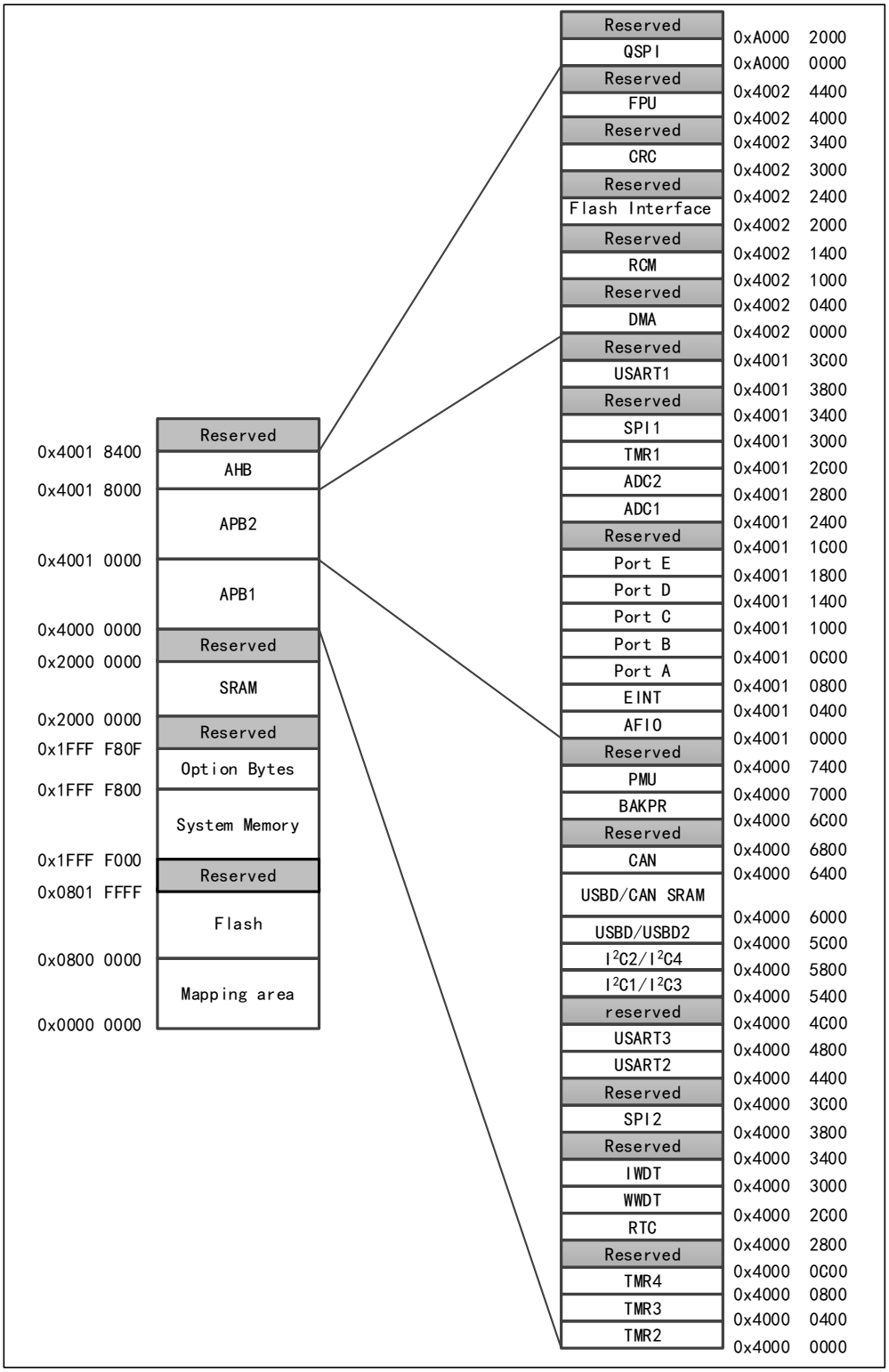



(1) The max frequency for APM32F103xB series AHB and high-speed APB is 96MHz;

(2) The max frequency for APM32F103xB series low-speed APB clock is 48MHz.

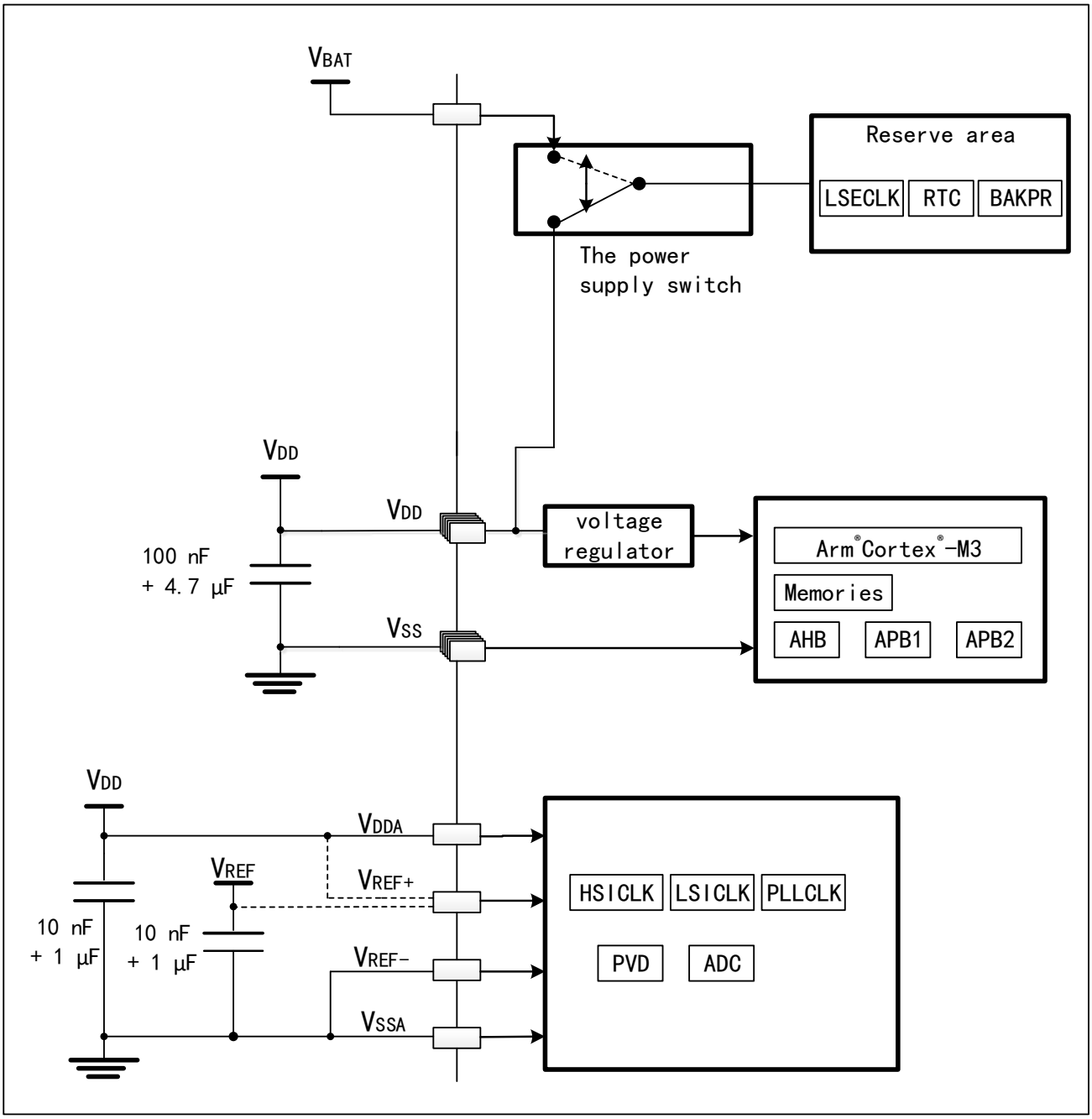
## 4.5. Address Mapping

Figure 7. APM32F103xB Series Address Mapping Diagram



## 4.6. Power Supply Scheme

Figure 8. Power Supply Scheme



# 5. Electrical Features

## 5.1. Parameter Conditions

All voltage parameters are referenced to VSS unless otherwise specified

### 5.1.1. Maximum and Minimum Values

Unless otherwise stated, all minimum and maximum values are guaranteed on the production line by testing 100% of the product at ambient temperature $T_A$=25°C under worst ambient temperature, supply voltage and clock frequency conditions.

Take notes in every table that the data got for passing the comphensive evaluation, design simulation or process features will not be tested on production lines. Basing on the comprehensive evaluation and sample tested, the minimum and maximum values come from the average value's plus or subtract its triple value on the standard distribution (average ±3∑).

### 5.1.2. Typical Value

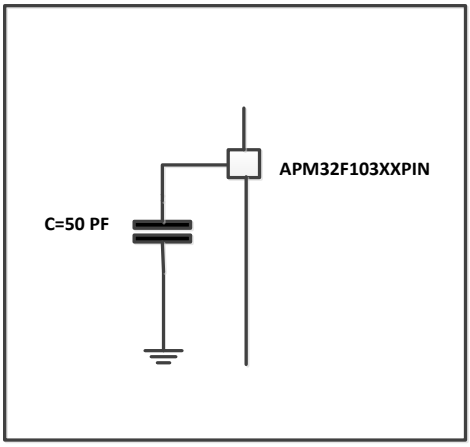
Typical data is based on $T_A$ =25°C and $V_{DD}$ =3.3V (2 V ≤ $V_{DD}$ ≤ 3.3 V voltage range) unless otherwise stated. These data are for design guidance only.

### 5.1.3. Typical Curve

Typical curves are for design guidance only and are not tested unless otherwise stated.

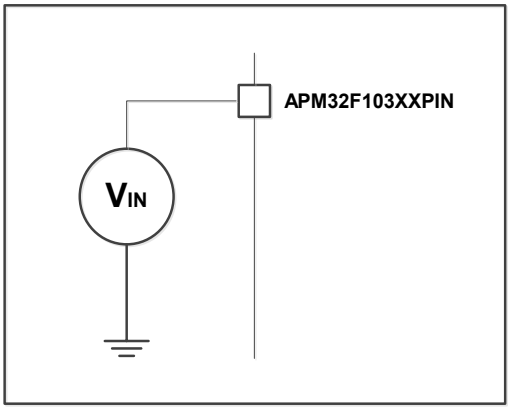
### 5.1.4. Load Capacitance

Figure 9. Load Conditions When Measuring Pin Parameters



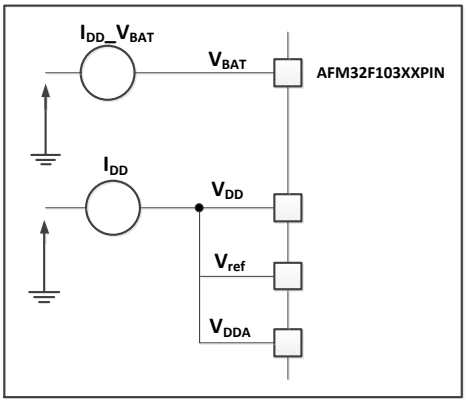

A: load capacitance

Figure 10. Pin Input Voltage Measurement Scheme




B: Pin Input Voltage

Figure 11. Current Consumption Measurement Scheme




C: Current consumption measurement($I_{DD}$+$V_{ref}$)

## 5.2. Absolute Maximum Ratings

Loads applied to the device may cause permanent damage to the device if the absolute maximum ratings are given in the maximum rated voltage Features and maximum rated current Features. This is just to give the maximum load that can be tolerated, and does not mean that the functionality of the device is functioning properly under these conditions. The reliability of device would be affected if it works under the maximum load conditions for a long Time.

### 5.2.1. Maximum Rated Voltage Features

Table 9. Maximum Rated Voltage Features

| Symbol | Description | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $V_{DD}$ - $V_{SS}$ | External main supply voltage (including $V_{DDA}$ and $V_{DD}$) (1) | -0.3 | 4.0 | V |
| $V_{IN}$ | Input voltage on 5V tolerant pins (2) | $V_{SS}$-0.3 | 5.5 | |
| | Input voltage on other pins(2) | $V_{SS}$-0.3 | $V_{DD}$ + 0.3 | |
| \| $\Delta V_{DDx}$ \| | Voltage difference between different supply pins | | 50 | mV |

| Symbol | Description | Minimum | Maximum | Unit |
|---|---|---|---|---|
| $\lvert V_{SSx}-V_{SS} \rvert$ | Voltage difference between different ground pins | | 50 | |

(1) All power ($V_{DD}$, $V_{DDA}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to a power supply within the external allowable range.

(2) If $V_{IN}$ does not exceed the maximum value, $I_{INJ(PIN)}$ will not exceed its limit. If $V_{IN}$ exceeds the maximum value, $I_{INJ(PIN)}$ must be externally limited to not exceed its maximum value. When $V_{IN} > V_{DD}$, there is a forward injection current; when $V_{IN}<V_{SS}$, there is a reverse injection current.

### 5.2.2. Maximum Rated Current Features

Table 10.Maximum Rated Current Features

| Symbol | Description | Maximum | Unit |
|---|---|---|---|
| $I_{VDD}$ | Total current (supply current) (1) went through the $V_{DD}/V_{DDA}$ power cord. | 150 | mA |
| $I_{VSS}$ | Total current (outflow current) (1) went through the $V_{SS}$ ground cord. | 150 | |
| $I_{IO}$ | Irrigation current on any I/O and control pins | 25 | |
| | Source current on any I/O and control pins | -25 | |
| $I_{INJ(PIN)}$ (2) (3) | Injection current of NRST pin | ±5 | |
| | Injection current of HSECLK's OSC_IN pin and LSECLK's OSC_IN pin | ±5 | |
| | Injection current of other pins | ±5 | |
| $\Sigma I_{INJ(PIN)}$(2) | Total injection current on all I/O and control pins (4) | ±25 | |

(1) All power ($V_{DD}$，$V_{DDA}$) and ground ($V_{SS}$，$V_{SSA}$) pins must always be connected to a power supply within the external allowable range.

(2) If $V_{IN}$ does not exceed the maximum value, $I_{INJ(PIN)}$ will not exceed its limit. If VIN exceeds the maximum value, $I_{INJ(PIN)}$ must be externally limited to not exceed its maximum value. When $V_{IN} > V_{DD}$, there is a forward injection current; when $V_{IN} < V_{SS}$, there is a reverse injection current.

(3) Reverse injection current can interfere with the analog performance of the ADC.

(4) When several I/O ports have injection current at the same Time, the maximum value of$\Sigma I_{INJ(PIN)}$ is the sum of the instantaneous absolute values of the forward injection current and the reverse injection current. These results are based on the calculation of the maximum value of $\Sigma I_{INJ(PIN)}$ on the four I/O port pins of the device.

### 5.2.3. Maximum Temperature Features

Table 11.Temperature Features

| Symbol | Description | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | -55 ~ + 150 | °C |
| $T_J$ | Maximum junction temperature | 150 | °C |

### 5.2.4. Maximum Ratings Electrical Sensitivity

**Electrostatic Discharge (ESD)**

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size is 3parts x(n+1) supply pins. The test is compliant with JS-001-2017/JS-002-2018 standard.

Table 12.ESD Absolute Maximum Ratings（1）

| Symbol | Ratings | Conditions | Maximum value (1) | Unit |
|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A$ = +25 °C, compliant with standard JS-001-2017 | 2000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charging device model) | $T_A$ = +25 °C, compliant with standard JS-002-2018 | 1000 | |

(1) The sample is measured by a third-party testing agency and is not tested in production

**Static Latch-up(LU)**

When running a simple application (controlling 2 LED flashes through I/O ports), the test sample is subjected to false electromagnetic interference until an error occurs, and the flashing LED indicating the error is for evaluating the latch performance. Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin The test is compliant with EIA/JESD78E latch-up standard.

Table 13.Static Latch（1）

| Symbol | Parameters | Conditions | Type |
|---|---|---|---|
| LU | Static latch | $T_A$ = +25 °C/105°C,compliant with standard EIA/JESD78E | CLASS Ⅱ A |

(1) The sample is measured by a third-party testing agency and is not tested in production.

## 5.3. Test Under the General Working Conditions

Table 14.General Working Conditions

| Symbol | Parameters | Conditions | Min value | Max value | Unit |
|---|---|---|---|---|---|
| $f_{HCLK}$ | Internal AHB clock frequency | | 0 | 96 | MHz |
| $f_{PCLK1}$ | Internal APB1 clock frequency | | 0 | 48 | |
| $f_{PCLK2}$ | Internal APB2 clock frequency | | 0 | 96 | |
| $V_{DD}$ | Standard working voltage | | 2 | 3.6 | V |
| $V_{DDA}$(1) | Analog operating voltage (ADC not used) | must be the same with $V_{DD}$(2) | 2 | 3.6 | V |
| | Analog operating voltage (ADC not used) | | 2.4 | 3.6 | |
| $V_{BAT}$ | Backup operating voltage | | 1.6 | 3.6 | V |
| TA | Ambient temperature range (temperature label 6) | Maximum power consumption | -40 | 105 | °C |
| | Ambient temperature range (temperature label 7) | Maximum power consumption | -40 | 105 | °C |
| TJ | Junction temperature range | | -40 | 150 | °C |

(1) When the ADC is used, refer to Chapter 5.2.16.

(2) It is recommended to power $V_{DD}$ and $V_{DDA}$ from the same source. A maximum difference of 300mV between $V_{DD}$ and $V_{DDA}$ can be tolerated during power-up and operation.

### 5.3.1. Embedded Reset and Power Control Block Features

Table 15.Embedded Reset and Power Control Block Features ($T_A$=25℃)（-40℃~+105℃）

| Symbol | Parameters | Conditions | Minimum Value | Typical Value | Maximum Value | Unit |
|---|---|---|---|---|---|---|
| $V_{PVD}$(3) | Programmable voltage detector level selection | PLS[2:0]=000 (rising edge) | 2.18 | 2.2 | 2.22 | V |
| | | PLS[2:0]=000 (falling edge) | 2.08 | 2.09 | 2.11 | V |
| | | PLS[2:0]=001 (rising edge) | 2.28 | 2.3 | 2.32 | V |
| | | PLS[2:0]=001 (falling edge) | 2.17 | 2.19 | 2.21 | V |
| | | PLS[2:0]=010 (rising edge) | 2.38 | 2.4 | 2.42 | V |
| | | PLS[2:0]=010 (falling edge) | 2.27 | 2.29 | 2.31 | V |
| | | PLS[2:0]=011 (rising edge) | 2.48 | 2.5 | 2.52 | V |
| | | PLS[2:0]=011 (falling edge) | 2.37 | 2.39 | 2.41 | V |
| | | PLS[2:0]=100 (rising edge) | 2.58 | 2.6 | 2.62 | V |
| | | PLS[2:0]=100 (falling edge) | 2.47 | 2.49 | 2.51 | V |
| | | PLS[2:0]=101 (rising edge) | 2.67 | 2.69 | 2.72 | V |
| | | PLS[2:0]=101 (falling edge) | 2.57 | 2.59 | 2.61 | V |
| | | PLS[2:0]=110 (rising edge) | 2.77 | 2.8 | 2.82 | V |
| | | PLS[2:0]=110 (falling edge) | 2.66 | 2.68 | 2.71 | V |
| | | PLS[2:0]=111 (rising edge) | 2.86 | 2.89 | 2.91 | V |
| | | PLS[2:0]=111 (falling edge) | 2.76 | 2.79 | 2.81 | V |
| $V_{PVDhyst}$(2) | PVD hysteresis | | | 107 | | mV |
| $V_{POR/PDR}$ | Power on/power down reset threhold | Falling edge | 1.87(1) | 1.89 | 1.91 | V |
| | | Rising edge | 1.92 | 1.94 | 1.96 | V |
| $V_{PDRhyst}$ (2) | PVD hysteresis | | | 50 | | mV |
| $T_{RSTTEMPO}$ | Reset Duration | | 0.9 | | 2.4 | ms |

(1) The product feature is guaranteed from design down to the minimum VPOR/PDR value.

(2) It is guaranteed from design, and is not tested in production.

(3) It is derived from a comprehensive evaluation and is not tested in production.

### 5.3.2. Built-in Reference Voltage Features Test

Table 16.Built-in Reference Voltage

| Symbol | Parameters | Conditions | Minimum Value | Typical Value | Maximum Value | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT}$(1) | Internal reference voltage | -40°C < $T_A$ < +105°C $V_{DD}$= 2-3.6 V | 1.198 | 1.210 | 1.223 | V |
| $T_{S\_vrefint}$(2) | ADC sampling Time | | | 5.1 | 17.1 | μs |

| Symbol | Parameters | Conditions | Minimum Value | Typical Value | Maximum Value | Unit |
|---|---|---|---|---|---|---|
| | when reading the internal reference voltage | | | | | |
| $V_{REFINT}$ | Variation of the built-in reference voltage in full temperature range | $V_{DD}$=3V±10mV | | | 20 | mV |
| $T_{Coeff}$ | | | | | 126 | ppm/℃ |

(1) Data was derived from a comprehensive evaluation and is not tested in production.

(2) It is guaranteed from design, and is not tested in production.

### 5.3.3. Supply Current Features

The current values in the operating modes given in this section are measured by executing Dhrystone 2.1, the compilation environment is Keil V5, and the compilation optimization level is L3.

**Max Current Consumption**

The microcontroller is under the following conditions:

- All I/O pins are in input mode and are connected to a static level –$V_{DD}$ or $V_{SS}$ (no load).
- All peripherals are turned off unless otherwise stated.
- The access time of the flash memory is adjusted to the frequency $f_{HCMU}$ (0~24MHz - 0 wait cycles, 24~48MHz - 1 wait cycle, 48~72MHz - 2 wait cycles, 72~96MHz - 3 wait cycles).
- The instruction prefetch function is turned on (hint: this setting must be made before the clock setting and bus division).
- When the peripheral is turned on: $fp_{CMU1} = f_{HCMU}/2$ ，$fp_{CMU2} = f_{HCMU}$.

Table 17. Run-mode Current Consumption, Code with Data Processing Running From Internal Flash

| Symbol | Parameters | Conditions | $f_{HCLK}$ | Maximum Value(1) | Unit |
|---|---|---|---|---|---|
| | | | | $T_A$=105°C , $V_{DD}$=3.6 V | |
| $I_{DD}$ | Supply current in operating mode | External clock (2), enabling all peripherals | 96 MHz | 31.05 | mA |
| | | | 72MHz | 25.78 | |
| | | | 48MHz | 19.82 | |
| | | | 36MHz | 15.19 | |
| | | | 24MHz | 11.47 | |
| | | | 16MHz | 8.01 | |
| | | | 8MHz | 4.41 | |
| | | External clock (2), turn off all peripherals | 96 MHz | 20.03 | |
| | | | 72MHz | 17.60 | |
| | | | 48MHz | 14.24 | |
| | | | 36MHz | 10.89 | |
| | | | 24MHz | 8.65 | |
| | | | 16MHz | 6.30 | |
| | | | 8MHz | 3.54 | |

(1) Data was derived from a comprehensive evaluation and is not tested in production.

(2) When the external clock is 8MHz and $f_{HCMU}$ >8MHz, it enables PLL.

Table 18.Run-mode Current Consumption, Code with Data processing Running From Internal RAM

| Symbol | Parameters | Conditions | $f_{HCLK}$ | Maximum Value(1) | Unit |
|---|---|---|---|---|---|
| | | | | $T_A$=105°C , $V_{DD}$=3.6 V | |
| $I_{DD}$ | Supply current in operating mode | External clock(2), enabling all peripherals | 96 MHz | 27.82 | mA |
| | | | 72MHz | 21.82 | |
| | | | 48MHz | 14.39 | |
| | | | 36MHz | 11.02 | |
| | | | 24MHz | 7.69 | |
| | | | 16MHz | 5.45 | |
| | | | 8MHz | 3.20 | |
| | | External clock (2), turn off all peripherals | 96 MHz | 16.85 | |
| | | | 72MHz | 12.74 | |
| | | | 48MHz | 8.86 | |
| | | | 36MHz | 6.87 | |
| | | | 24MHz | 4.92 | |
| | | | 16MHz | 3.66 | |
| | | | 8MHz | 3.19 | |

(1) Data was derived from a comprehensive evaluation and is not tested in production.

(2) When the external clock is 8MHz and $f_{HCMU}$ >8MHz, it enables PLL.

Table 19.Maximum Current Consumption in Sleep Mode, Code Runs from Flash or RAM

| Symbol | Parameters | Conditions | $f_{HCLK}$ | Maximum Value(1) $T_A$ =105°C , $V_{DD}$=3.6 V | Unit |
|---|---|---|---|---|---|
| $I_{DD}$ | Static Current during Sleep Mode | External clock (2), enabling all peripherals | 96 MHz | 17.39 | mA |
| | | | 72MHz | 13.32 | |
| | | | 48MHz | 9.14 | |
| | | | 36MHz | 7.11 | |
| | | | 24MHz | 5.07 | |
| | | | 16MHz | 3.69 | |
| | | | 8MHz | 2.31 | |
| | | External clock (2), turn off all peripherals | 96 MHz | 5.07 | |
| | | | 72MHz | 4.06 | |
| | | | 48MHz | 3.02 | |
| | | | 36MHz | 2.46 | |
| | | | 24MHz | 1.99 | |
| | | | 16MHz | 1.62 | |
| | | | 8MHz | 1.31 | |

(1) Data was derived from a comprehensive evaluation and is not tested in production.

(2) When the external clock is 8MHz and $f_{HCMU}$ >8MHz, it enables PLL.

Table 20.Maximum Current Consumption in Stop Mode and Standby Mode

| Symbol | Parameters | Conditions | Maximum Value(1) | Unit |
|---|---|---|---|---|
| | | | $T_A$=105°C，$V_{DD}$=3.6 V | |
| $I_{DD}$ | Supply current in stop mode | Regulator in run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF(no independent watchdog) | 94.19 | μA |
| | | Regulator in low-power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF(no independent watchdog) | 79.18 | |
| | Supply current in standby mode | Low-speed internal RC oscillator and independent watchdog ON | 17 | |
| | | Low-speed internal RC oscillator is on, independent watchdog OFF | 16.82 | |
| | | Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF | 15.89 | |
| $I_{DD\_VBAT}$ | Supply current in the backup area | Low-speed oscillator and RTC ON | 3.0 | |

(1) Data was derived from a comprehensive evaluation and is not tested in production.

**Typical Current Consumption**

The microcontroller is under the following conditions:

- All I/O pins are in input mode and are connected to a static level –$V_{DD}$ or $V_{SS}$ (no load).
- All peripherals are turned off unless otherwise stated.
- The access time of flash is adjusted to the frequency $f_{HCMU}$ (0~24MHz-0 wait cycles, 24~48MHz-1 wait cycle, 48~72MHz-2 wait cycles,96MHz-3 wait cycles).
- The instruction prefetch function is turned on (hint: this setting must be made before the clock setting and bus division).

When the peripheral is turned on: $f_{pCMU1} = f_{HCMU}/2$ ， $f_{pCMU2} = f_{HCMU}$.

Table 21.Run-mode current consumption, code with data processing running from internal Flash

| Symbol | Parameter | $f_{HCMU}$ | Typical Value(1) | | Unit |
|---|---|---|---|---|---|
| | | | $T_A$=25°C,$V_{DD}$=3.3V | | |
| | | | External clock(2), enables all peripherals | External clock (2), turn off all peripherals | |
| $I_{DD}$ | Supply current in operation mode | 96 MHz | 30.94 | 19.37 | mA |
| | | 72MHz | 25.47 | 17.22 | |
| | | 48MHz | 19.35 | 14.08 | |
| | | 36MHz | 14.95 | 10.67 | |
| | | 24MHz | 11.17 | 8.32 | |
| | | 16MHz | 7.72 | 6.01 | |
| | | 8MHz | 4.25 | 3.28 | |

(1) Data was derived from comprehensive evaluation and is not tested in production.

(2) When the external clock is 8MHz and $f_{HCMU}$ >8MHz, it enables PLL.

Table 22.Run-mode current consumption, code with data processing running from internal RAM

| Symbol | Parameter | $f_{HCMU}$ | Typical Value(1) | | Unit |
|---|---|---|---|---|---|
| | | | TA=25°C,VDD=3.3V | | |
| | | | External clock(2), enables all peripherals | External clock (2), turn off all peripherals | |
| $I_{DD}$ | Supply current in operation mode | 96 MHz | 27.53 | 16.42 | mA |
| | | 72MHz | 20.78 | 12.51 | |
| | | 48MHz | 14.43 | 8.74 | |
| | | 36MHz | 11.02 | 6.61 | |
| | | 24MHz | 7.65 | 4.68 | |
| | | 16MHz | 5.36 | 3.37 | |
| | | 8MHz | 3.08 | 3.10 | |

(1) Data was derived from comprehensive evaluation and is not tested in production.

(2) When the external clock is 8MHz and $f_{HCMU}$ >8MHz, it enables PLL.

Table 23.Typical current consumption in sleep mode, code running from Flash or RAM

| Symbol | Parameter | $f_{HCMU}$ | Typical Value(1) | | Unit |
|---|---|---|---|---|---|
| | | | TA=25°C,VDD=3.3V | | |
| | | | External clock(2), enables all peripherals | External clock (2), turn off all peripherals | |
| $I_{DD}$ | Supply current in sleep mode | 96 MHz | 17.18 | 5.16 | mA |
| | | 72MHz | 13.03 | 3.92 | |
| | | 48MHz | 9.11 | 2.88 | |
| | | 36MHz | 7.06 | 2.36 | |
| | | 24MHz | 5.01 | 1.85 | |
| | | 16MHz | 3.67 | 1.52 | |
| | | 8MHz | 2.25 | 1.19 | |

(1) Data was derived from comprehensive evaluation and is not tested in production.

(2) When the external clock is 8MHz and $f_{HCMU}$ >8MHz, it enables PLL.

Table 24.Typical current Consumption in Stop Mode and Standby Mode

| Symbol | Parameters | Conditions | Typical Value（$T_A$ =25°C） | | | Unit |
|---|---|---|---|---|---|---|
| | | | $V_{DD}$ =2.4 V | $V_{DD}$ =3.3 V | $V_{DD}$ =3.6 V | |
| $I_{DD}$ | Supply current in stop mode | Regulator in run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF(no independent watchdog) | 22.68 | 24.02 | 24.22 | μA |
| | | Regulator in low-power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF(no independent watchdog) | 10.91 | 11.88 | 11.93 | |
| | Supply current in standby mode | Low-speed internal RC oscillator and independent watchdog ON | 3.61 | 5.0 | 5.49 | |
| | | Low-speed internal RC oscillator is on, independent watchdog OFF | 3.51 | 4.86 | 5.32 | |
| | | Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF | 2.91 | 3.95 | 4.30 | |
| $I_{DD\_VBAT}$ | Supply current in the backup area | Low-speed oscillator and RTC ON | 1.1 | 1.4 | 1.4 | |

(1) Data was derived from a comprehensive evaluation and is not tested in production

### 5.3.4. External Clock Source Features

**High-speed External Clock Generated From Crystal/Ceramic Resonator**

The high-speed external(HSECLK) clock can be supplied with a 4 to 16MHz crystal\ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in Table 25. In the application, the resonator and the load capacitors have to be placed as closed as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. For detailed parameters (frequency, package, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer.

Table 25.HSECLK 4~16MHz Oscillator Features(1)(2)

| Symbol | Parameters | Conditions | Minimum Value | Typical Value | Maximum Value | Unit |
|---|---|---|---|---|---|---|
| $f_{OSC\_IN}$ | Oscillator Frequency: | | 4 | 8 | 16 | MHz |
| $R_F$ | Feedback Resistance | | | 300 | | kΩ |
| $C_{L1}$& $C_{L2}$(3) | Recommended load capacitance and corresponding crystal serial impedance (RS) (4) | RS = 30kΩ | | 30 | | pF |
| $i_2$ | HSECLK drive current | $V_{DD}$=3.3V，$V_{IN}$=$V_{SS}$ 30pF load | | | 1.1 | mA |
| $t_{SU(HSECLK)}$(5) | Startup Time | $V_{DD}$ is stable | | 1.33 | | ms |

(1) The features parameters of the resonator are given by the crystal/ceramic resonator manufacturer.

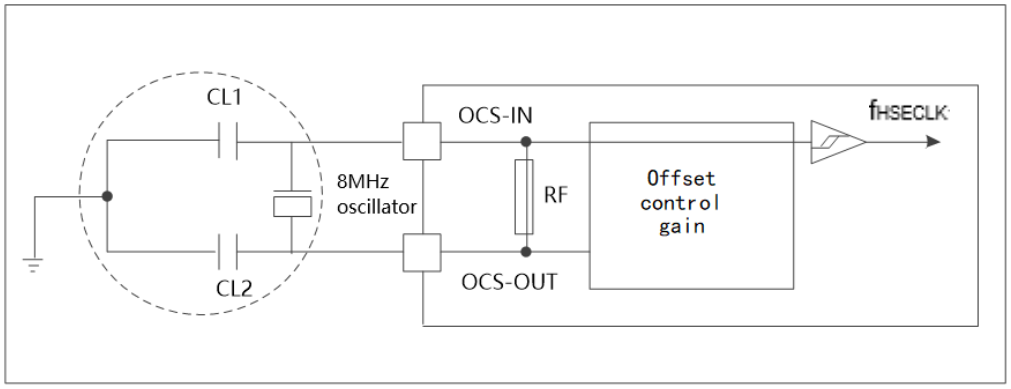
(2) It is derived from a comprehensive evaluation and is not tested in production.

(3) For $C_{L1}$ and $C_{L2}$, it is recommended to use high quality ceramic capacitors (typically) between 5pF and 25pF for high frequency applications. Select the capacitor value to meet the requirements of the crystal or resonator. Usually $C_{L1}$ and $C_{L2}$ have the same parameters. Crystal manufacturers typically give the parameters of the load capacitance in a serial combination of $C_{L1}$ and $C_{L2}$. When selecting $C_{L1}$ and $C_{L2}$, the capacitive reactance of the PCB and MCU pins should be taken into account (the pin and PCB capacitance can be roughly esTMRated at 10pF).

(4) Relatively low RF resistance provides protection against problems caused by changes in leakage and bias conditions when used in wet conditions. However, if the MCU is used in a harsh wet environment, this factor needs to be taken into account when designing.

(5) $t_{SU(HSECLK)}$ is the start-up time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured using a standard crystal resonator, which may vary greatly depending on the crystal manufacturer.

Figure 12. Typical application of 8MHz crystal oscillator




**Low-speed External Clock Generated From the Crystal/Ceramic Resonator**

The low-speed external(LSECLK) clock can be supplied with a 32.768kHz crystal\ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in table 26.In the application, the resonator and load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. For detailed parameters (frequency, package, accuracy, etc.) of the crystal resonator, please consult the corresponding manufacturer.

Table 26.LSECLK Oscillator Features ($f_{LSECLK}$ =32.768KHz) (1)

| Symbol | Parameters | Conditions | Minimum Value | Typical Value | Maximum Value | Unit |
|---|---|---|---|---|---|---|
| $f_{OSC\_IN}$ | Oscillator frequency | | | 32.768 | | KHz |
| RF | Feedback Resistance | | | 7 | | MΩ |
| $C_{L1}$ & $C_{L2}$(2) | Recommended load capacitance and corresponding crystal serial impedance ($R_S$) (3) | $R_S$ = 30kΩ | | | 15 | pF |
| $i_2$ | LSECLK drive current | $V_{DD}$ = 3.3V, $V_{IN}$=$V_{SS}$ | | | 1.4 | μA |
| $t_{SU(LSECLK)}$(4) | Start Time | $V_{DD}$ is stable | | 2.75 | | s |

(1) Data was derived from a comprehensive evaluation and is not tested in production.

(2) See the tips and warnings section below this table.

(3) Use a high quality oscillator with a small $R_S$ value (such as MSIV-TIN32.768kHz) to optimize current consumption. Please consult the crystal manufacturer for details.

(4) $t_{SU(HSECLK)}$ is the start-up time measured from the moment it is enabled (by software) to a

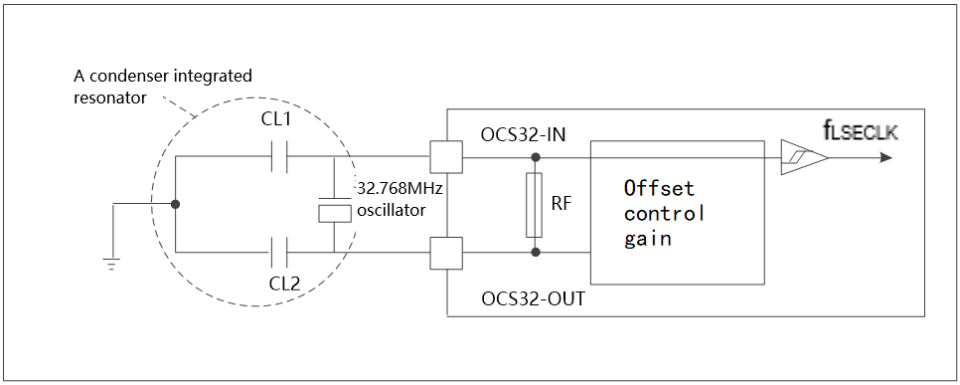
stabilized 8 MHz oscillation is reached. This value is measured using a standard crystal resonator, which may vary greatly depending on the crystal manufacturer

**Tip:** For $C_{L1}$ and $C_{L2}$, it is recommended to use a high quality ceramic capacitor between 5pF and 15pF and select the capacitance value to meet the requirements of the crystal or resonator. Usually $C_{L1}$ and $C_{L2}$ have the same parameters. Crystal manufacturers typically give the parameters of the load capacitance in a serial combination of $C_{L1}$ and $C_{L2}$. Load capacitance CL has the following formula:CL- $C_{L1}$ x $C_{L2}$/( $C_{L1}$ + $C_{L2}$) + $C_{stray}$ where $C_{stray}$ is the pin capacitance and board or trace PCB-related capacitance, Typically, it is between 2 pF and 7 pF.

**Warning:** To avoid exceeding the maximum value of $C_{L1}$ and $C_{L2}$ (15 pF) it is strongly recommended to use a resonator with a load capacitance CL≤7pF. Never use a resonator with a load capacitance of 12.5 pF.

Example: if you choose a resonator with a load capacitance of CL=6 pF, and $C_{stray}$ = 2 pF, then $C_{L1}$= $C_{L2}$ =8 pF

Figure 13. Typical application of 32.768MHz crystal oscillator




## 5.3.5. Internal Clock Source Features

### High Speed Internal (HSICLK) RC Oscillator Tes

Table 27.HSICLK Oscillator Features(1)

| Symbol | Parameters | Conditions | | Minimum Value | Typical Value | Maximum Value | Unit |
|---|---|---|---|---|---|---|---|
| $f_{HSICLK}$ | Frequency | | | | 8 | | MHz |
| $ACC_{HSICLK}$ | HSICLK oscillator accuracy | Factory calibration | $T_A$=25°C<br>$V_{DD}$ = 3.3V | 1 | | 1 | % |
| | | | $T_A$=-40~105°C<br>$V_{DD}$ = 2-3.6V | -2.63 | | 3.56 | % |
| | | | $T_A$ =25°C<br>$V_{DD}$ = 2-3.6V | -0.88 | | 3.28 | % |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | User calibration | | -1 | | 1 | |
| $t_{SU(HSICLK)}$ | HSICLK oscillator startup Time | $V_{DD}$ = 3.3V $T_A$ =-40~105°C | | 1.73 | | 2.12 | μs |
| $I_{DD(HSICLK)}$ | HSICLK oscillator power consumption | $V_{DD}$ = 3.6V $T_A$ =-40~105°C | | | | | μA |

(1) Data was derived from a comprehensive evaluation and is not tested in production

**Low Speed Internal (LSICLK) RC Oscillator Test**

Table 28.LSICLK Oscillator Features (1)

| Symbol | Parameters | Minimum Value | Typical Value | Maximum Value | Unit |
|---|---|---|---|---|---|
| $f_{LSICLK}$ | Frequency ($V_{DD}$ = 2-3.6V，$T_A$ = -40~105°C) | 41 | 40 | 50 | KHz |
| $t_{SU(LSICLK)}$ | LSICLK oscillator startup Time ($V_{DD}$ = 3.3V，$T_A$ = -40~105°C) | | | 39 | μs |
| $I_{DD(LSICLK)}$ | LSICLK oscillator power consumption ($V_{DD}$ = 3.6V，$T_A$ = -40~105°C) | | 1 | 1.5 | μA |

（1）Data was derived from a comprehensive evaluation and is not tested in production.

**Wake Up Time in Low Power Mode**

The Time values in the table are all a wake-up clock source from an 8MHz HSICLK RC oscillator and measured during its wake-up phase. The wake-up clock source is deteremined by current working mode:

- Stop or standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock set when entering sleep mode

Table 29.Wake Up Time in Low Power Mode

| Symbol | Parameters | Typical Value | Unit |
|---|---|---|---|
| $t_{WUSLEEP}$(1) | Wake up from sleep mode | 1.2 | μs |
| $t_{WUSTOP}$(1) | Wake up from stop mode (regulator is in running-mode) | 3.6 | μs |
| | Wake-up from stop mode (regulator is low power mode) | 6 | |
| $t_{WUSTDBY}$(1) | Wake-up from standby mode | 32 | μs |

(1) The wakeup Times are measured from the wakeup event to the point in which the user

application code reads the first instruction

### 5.3.6. PLL Features

Table 30.PLL Features

| Symbol | Parameters | Value | | | Unit |
|---|---|---|---|---|---|
| | | Minimum Value | Typical Value | Maximum Value (1) | |
| $f_{PLL\_IN}$ | PLL Input clock (2) | 2 | 8 | 25 | MHz |
| | Input Clock Duty Cycle | 40 | | 60 | % |
| $f_{PLL\_OUT}$ | PLL multiplier output clock ($V_{DD}$ = 3.3V，$T_A$ = -40~105°C） | 16 | | 96 | MHz |
| $t_{LOCK}$ | PLL lock Time | | | 130 | μs |

(1) Data was derived from a comprehensive evaluation and is not tested in production.

(2) Note that the appropriate multiplication factor is used so that the PLL input clock frequency is consistent with the range determined by $f_{PLL\_OUT}$.

### 5.3.7. Memory Features

**FLASH Memory**

Table 31.FLASH Memory Features (1)

| Symbol | Parameters | Conditions | Minimum Value | Typical Value | Maximum Value | Unit |
|---|---|---|---|---|---|---|
| $t_{prog}$ | 16-bit programming Time | $T_A$ = -40~105°C $V_{DD}$=2.4~3.6V | 17.8 | 18.6 | 19.5 | μs |
| $t_{ERASE}$ | Page (1K bytes) erase Time | $T_A$ = -40~105°C $V_{DD}$=2.4~3.6V | 1.34 | 1.42 | 1.51 | ms |
| $t_{ME}$ | Whole erase Time | $T_A$ = 25°C $V_{DD}$=3.3V | | | 6.5 | ms |
| $V_{prog}$ | Programmable voltage | $T_A$ = -40~105°C | 2.0 | 3.3 | 3.6 | V |

(1) Data was derived from a comprehensive evaluation and is not tested in production

Table 32.FLASH Memory Life and Data Retention Period

| Symbol | Parameters | Conditions | Minimum Value | Typical Value | Maximum Value | Unit |
|---|---|---|---|---|---|---|
| $N_{END}$ | Number of erase cycles | $T_A$ =-40~85℃ | 100 | | | Thousand Times cycle |

| | | | | | | |
|---|---|---|---|---|---|---|
| $t_{RET}$ | Data Retention Period | $T_A$ = 55°C | 20 | | | Years |

(1) Data was derived from a comprehensive evaluation and is not tested in production

### 5.3.8. I/O Ports Features

**Input/Output Static Features**

Table 33.I/O Static Features (Test conditions $V_{CC}$=2.7-3.6V, $T_A$ = -40~105°C)

| Symbol | Parameters | Conditions | Minimum Value | Typical Value | Maximum Value | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Low level input voltage | TTL port | -0.5 | | 0.8 | V |
| $V_{IH}$ | Standard I/O pin, input high level voltage | | 2 | | $V_{DD}$+0.5 | |
| | FT I/O pin(1), input high level voltage | | 2 | | 5.5 | |
| $V_{IL}$ | Input low level voltage | CMOS port | -0.5 | | $0.3V_{DD}$ | |
| $V_{IH}$ | Input high level voltage | | $0.7V_{DD}$ | | $V_{DD}$+0.5 | |
| $V_{hys}$ | Standard I/O Schmitt trigger voltage hysteresis(2)) | | 150 | | | mV |
| | FT I/O Schmitt trigger voltage hysteresis(2) | | $5\%V_{DD}$ | | | mV |
| $I_{lkg}$ | Input leakage current(3) | $V_{SS} \le V_{IN} \le V_{DD}$ Standard I/O port | | | ±1 | μA |
| | | $V_{IN}$ = 5V， I/O FT | | | 1 | |
| $R_{PU}$ | Weak pull-up equivalent resistance(4) | $V_{IN} = V_{SS}$ | 32 | 40 | 49 | kΩ |
| $R_{PD}$ | Weak pull-down equivalent resistance (4) | $V_{IN} = V_{DD}$ | 32 | 40 | 49 | kΩ |
| $C_{IO}$ | I/O pin capacitance | | | 5 | | pF |

(1) FT = 5V tolerant. To withstand voltages above $V_{DD}$ +0.3, the internal pull-up or pull-down resistors must be turned off.

(2) The hysteresis voltage of the Schmitt trigger switch level is derived from a comprehensive evaluation and is not tested in production.

(3) If there is reverse current sinking on adjacent pins, the leakage current may be higher than the maximum.

(4) The pull-up resistor is designed to be implemented as a true resistor in series with a

controllable PMOS/NMOS switch

**Output Drive Current Test**

The GPIO (General Purpose Input/Output Port) can sink or output up to ±8mA and can sink up to ±20mA ($V_{OL}$/$V_{OH}$ reduction). In user applications, the number of I/Os capable of driving current must be limited so that the current consumed cannot exceed the absolute maximum rating:

- The sum of the currents sourced by all the I/O on $V_{DD}$, plus the maximum Run consumption of the MCU sourced on $V_{DD}$, cannot exceed the absolute maximum rating $I_{VDD}$.
- The sum of the currents sunk by all the I/O on $V_{SS}$, plus the maximum Run consumption of the MCU sunk on $V_{SS}$, cannot exceed the absolute maximum rating $I_{VSS}$.

**Output Voltage Test**

Table 34.Output Voltage Features (test conditions $V_{CC}$=2.7-3.6V,$T_A$= -40~105°C)

| Symbol | Parameters | Conditions | Minimum Value | Maximum Value | Unit |
|---|---|---|---|---|---|
| $V_{OL}^{(1)}$ | Output low level, when 8 pins simultaneously sink current | TTL port, $I_{IO}$= +8mA 2.7V < $V_{DD}$ < 3.6V | | 0.4 | V |
| $V_{OH}^{(2)}$ | Output high level, when 8 pins simultaneously output current | | $V_{DD}$ -0.4 | | |
| $V_{OL}^{(1)}$ | Output low level, when 8 pins simultaneously sink current | CMOS port, $I_{IO}$= +8mA 2.7V < $V_{DD}$ < 3.6V | | 0.4 | V |
| $V_{OH}^{(2)}$ | Output high level, when 8 pins simultaneously output current | | 2.4 | | |
| $V_{OL}^{(1)(3)}$ | Output low level, when 8 pins simultaneously sink current | $I_{IO}$= +20mA 2.7V < $V_{DD}$ < 3.6V | | 1.3 | V |
| $V_{OH}^{(2)(3)}$ | Output high level, when 8 pins simultaneously output current | | $V_{DD}$ -1.3$^{(4)}$ | | |

(1) The current $I_{IO}$ absorbed by I/O must always follow the absolute maximum rating requirements, while the sum of the $I_{IO}$ s (all I/O and control pins) must not exceed $I_{VSS}$.

(2) The current $I_{IO}$ of the I/O output must always follow the absolute maximum rating requirements, while the sum of the $I_{IO}$ s (all I/O and control pins) must not exceed $I_{VDD}$.

(3) Data was derived from a comprehensive evaluation and is not tested in production.

(4) The driving capability of PC13-15 is not included in this item. The other PC port specifications are in the voltage range of 3.3V < $V_{DD}$ < 3.6V.

**Input and Output AC Features ($T_A$= 25°C)**

Table 35.Input and Output AC Features

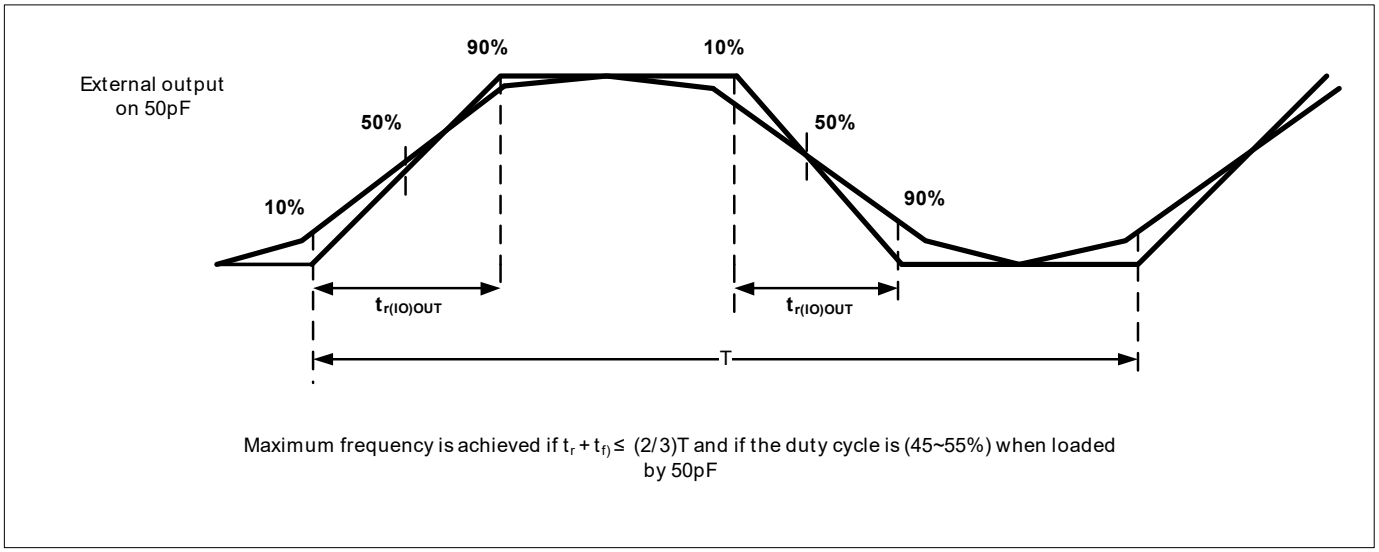
| MODEx[1:0] Configuration | Symbol | Parameters | Conditions | Minimum value | Maximum value | Unit |
|---|---|---|---|---|---|---|
| 10 (2MHz) | $f_{max(IO)out}$ | Max frequency(2) | $C_L$ = 50 pF, $V_{DD}$ = 2~3.6V | | 2 | MHz |
| | $t_{f(IO)out}$ | Output high to low fall Time | $C_L$ = 50 pF, $V_{DD}$ = 2~3.6V | | 50(3) | ns |
| | $t_{r\ (IO)out}$ | Output low to high rise Time | | | 50(3) | |
| 01 (10MHz) | $f_{max(IO)out}$ | Max frequency(2) | $C_L$ = 50 pF, $V_{DD}$ = 2~3.6V | | 10 | MHz |
| | $t_{f(IO)out}$ | Output high to low fall Time | $C_L$ = 50 pF, $V_{DD}$ = 2~3.6V | | 24(3) | ns |
| | $t_{r\ (IO)out}$ | Output low to high rise Time | | | 23 | |
| 11 (50MHz) | $f_{max(IO)out}$ | Max frequency(2) | $C_L$ = 30 pF, $V_{DD}$ = 2.7~3.6V | | 48 | MHz |
| | $t_{f(IO)out}$ | Output high to low fall Time | $C_L$ = 30 pF, $V_{DD}$ = 2.7~3.6V | | 7(3) | ns |
| | $t_{r\ (IO)out}$ | Output low to high rise Time | | | 5(3) | |

(1) The speed of the I/O port can be configured by MODEx[1:0].

(2) The maximum frequency is defined in the figure below.

(3) It is guaranteed from design and is not tested n production

Figure 14. Input and Output AC Features Definition



### 5.3.9. NRST Pins Features

The NRST pin input driver is implemented in a CMOS process that is connected to a permanent pull-up resistor, $R_{PU}$。

Table 36.NRST NRST Pin Features (Test condition $V_{CC}$=3.3V,$T_A$= -40~105°C )

| Symbol | Parameters | Conditions | Minimum Value | Typical Value | Maximum Value | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(NRST)}$(1) | NRST input low level voltage | | -0.5 | | 0.8 | V |
| $V_{IH(NRST)}$(1) | NRST input high level voltage | | 2 | | $V_{DD}$+0.5 | |
| $V_{hys(NRST)}$ | NRST Schmitt trigger voltage hysteresis | | | 300 | | mV |
| $R_{PU}$ | Weak pull-up equivalent resistance(2) | $V_{IN}$ = $V_{SS}$ | 32 | 40 | 49 | kΩ |

(1) Data is guaranteed from design, and is not tested in production.

(2) The pull-up resistor is implemented by a pure resistor in series with a turn-off PMOS/NMOS transistor. The PMOS/NMOS switch has a small resistance

### 5.3.10. Communication Interface

#### I²C Interface Features

Table 37.I²C Interface Features (Test conditions $V_{DD}$ = 3.3V，$T_A$= 25°C )

| Symbol | Parameters | Standard I²C(1) | | Fast I²C(1) (2) | | Unit |
|---|---|---|---|---|---|---|
| | | Minimum Value | Maximum Value | Minimum Value | Maximum Value | |
| $t_{w(SCLL)}$ | SCL clock low Time | 5.05 | | 1.72 | | μs |
| $t_{w(SCLH)}$ | SCL clock high Time | 4.94 | | 0.77 | | |
| $t_{su(SDA)}$ | SDA setup Time | 4532 | | 1216 | | ns |
| $t_{h(SDA)}$ | SDA hold Time | 0(3) | 503 | 0(4) | 459(3) | |
| $t_{r(SDA)}$ $t_{r(SCL)}$ | Rise Time for SDA and SCL | | 197 | | 190 | |
| $t_{f(SDA)}$ $t_{f(SCL)}$ | Fall Time for SDA and SCL | | 8 | | 9.8 | |
| $t_{h(STA)}$ | Start condition hold Time | 4.97 | | 0.82 | | μs |
| $t_{su(STA)}$ | Repeated start condition | 4.93 | | 0.81 | | |

| Symbol | Parameters | Standard I²C(1) | | Fast I²C(1) (2) | | Unit |
|---|---|---|---|---|---|---|
| | | Minimum Value | Maximum Value | Minimum Value | Maximum Value | |
| | setup Time | | | | | |
| $t_{su(STO)}$ | Stop condition setup Time | 4.91 | | 0.82 | | μs |
| $t_{w(STO:STA)}$ | Stop to Start condition Time (bus free) | 5.27 | | 4.02 | | μs |

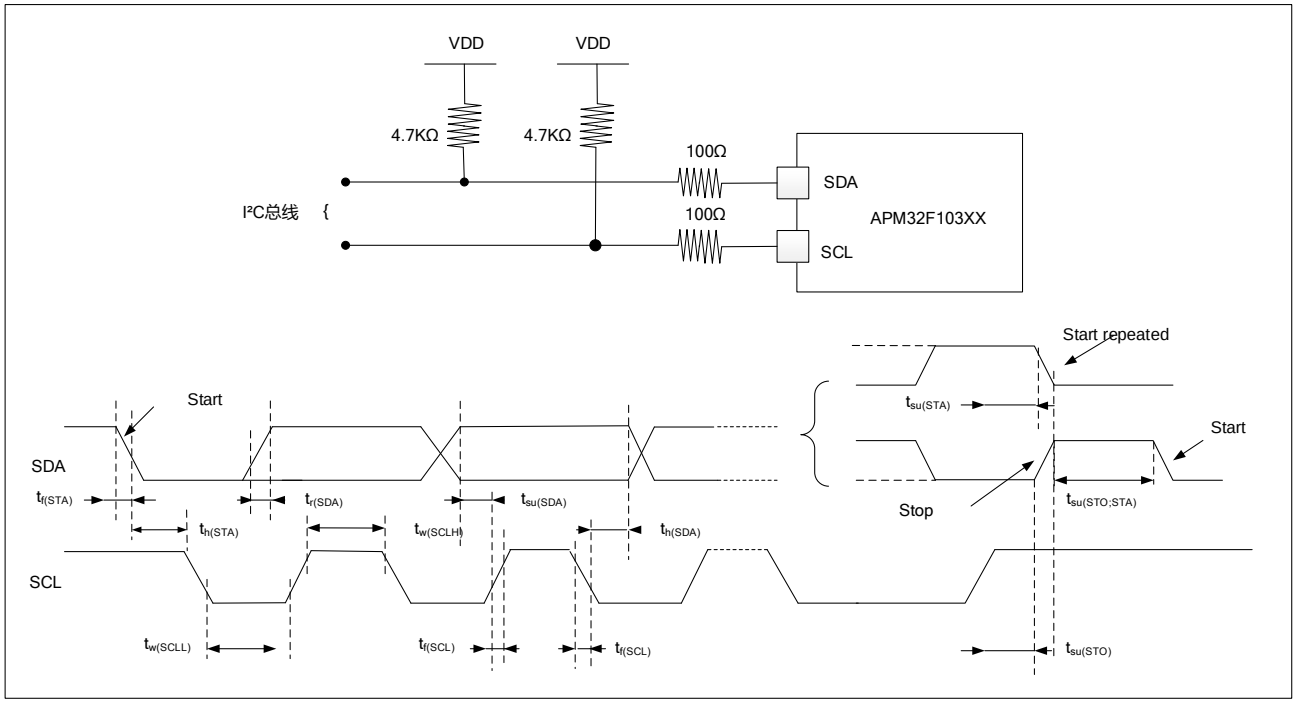
(1) It is guaranteed from design, and is not tested in production.

(2) For the bit to reach the maximum frequency of the standard mode I2C, fPCMU1 must be greater than 2MHz. To achieve the maximum frequency of fast mode I2C, fPCMU1 must be greater than 4MHz.

(3) If you do not want to stretch the low Time of the SCL signal, the maximum hold Time of the start condition must be met.

(4) In order to cross the undefined area of the falling edge of SCL, the SDA signal must be guaranteed to have a hold Time of at least 300 ns inside the MCU.

Figure 15. Bus AC Waveform and Measurement Circuit (1)




(1) Measured points are done at CMOS levels: 0.3 $V_{DD}$ and 0.7 $V_{DD}$.

**SPI Interface Features**

Table 38.SPI Features ($V_{DD}$= 3.3V，$T_A$=25°C)

| Symbol | Parameters | Conditions | Minimum Value | Maximum Value | Unit |
|---|---|---|---|---|---|
| $f_{SCK}$<br>$1/t_{c(SCK)}$ | SPI Clock Frequency | Master mode | | 18 | MHz |
| | | Slave Mode | | 18 | |
| $t_{r(SCK)}$<br>$t_{f(SCK)}$ | SPI clock rise and fall Times | Load capacitance: C=30pF | | 7.1 | ns |
| $t_{su(NSS)}$ (2) | NSS setup Time | Slave mode $f_{PCMU}$ = 36MHz | 111.4 | | ns |
| $t_{h(NSS)}$ (2) | NSS hold Time | Slave mode $f_{PCMU}$ = 36MHz | 55.6 | | ns |
| $t_{w(SCKH)}$(2)<br>$t_{w(SCKL)}$(2) | SCK high and low Time | Master mode, $f_{PCMU}$ = 36MHz，presc=4 | 55.1 | 55.9 | ns |
| $t_{su(MI)}$(2)<br>$t_{su(SI)}$(2) | Data input setup Time | Master mode | 10.9 | | ns |
| | | Slave mode | 21.3 | | |
| $t_{h(MI)}$(2)<br>$t_{h(SI)}$(2) | Data input hold Time | Master Mode | 35 | | ns |
| | | Slave Mode | 25 | | |
| $t_{a(SO)}$(2)(3) | Data output access Time | Slave mode, $f_{PCLK}$ = 20MHz | 6.5 | 8.7 | ns |
| $t_{dis(SO)}$(2)(4) | Data output disable Time | Slave mode | 12 | | ns |
| $t_{v(SO)}$(2)(1) | Data output valid Time | Slave mode (after enable edge) | | 19.3 | ns |
| $t_{v(MO)}$(2)(1) | Data output valid Time | Master mode (after enable edge) | | 7.6 | ns |
| $t_{h(SO)}$(2) | Data output hold Time | Slave mode (after enable edge) | 10.7 | | ns |
| $t_{h(MO)}$(2) | | Master mode (after enable edge) | 2 | | |

(1) The SPI1 feature of the remap needs further determination.

(2) It is derived from calculation and is not tested in production.

(3) The minimum value represents the minimum Time to drive the output, and the maximum value represents the maximum Time at which the data is valid.

(4) The minimum value represents the minimum Time to turn off the output, and the maximum value represents the maximum Time to place the data line in a high impedance state.

Figure 16. SPI Timing Diagram - Slave Mode and CPHA=0

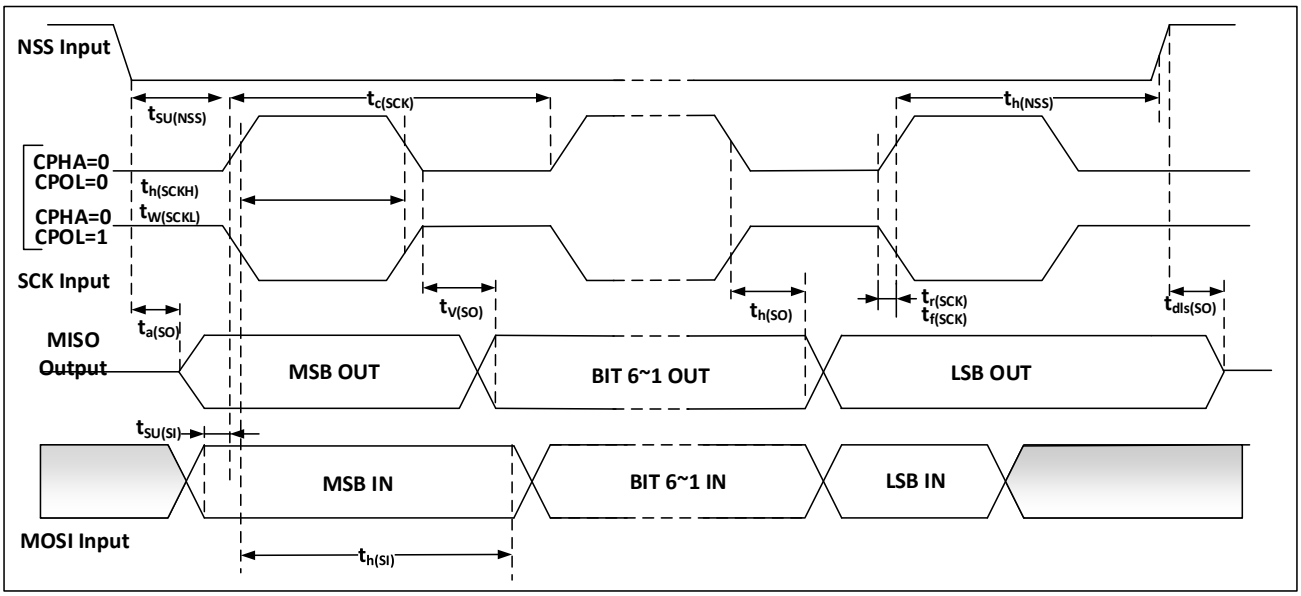
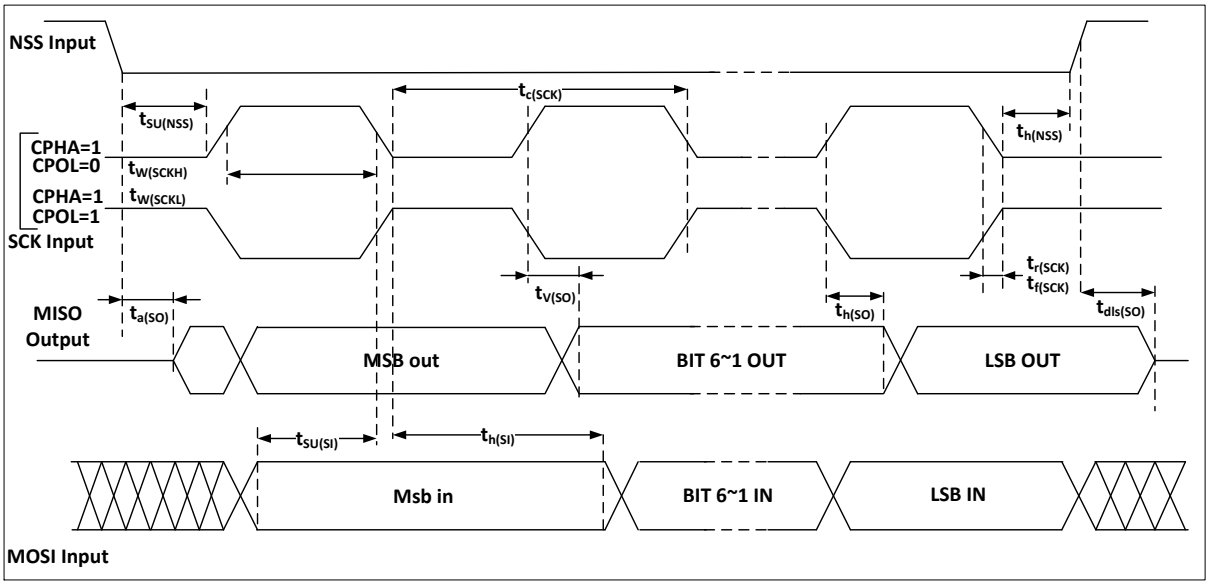
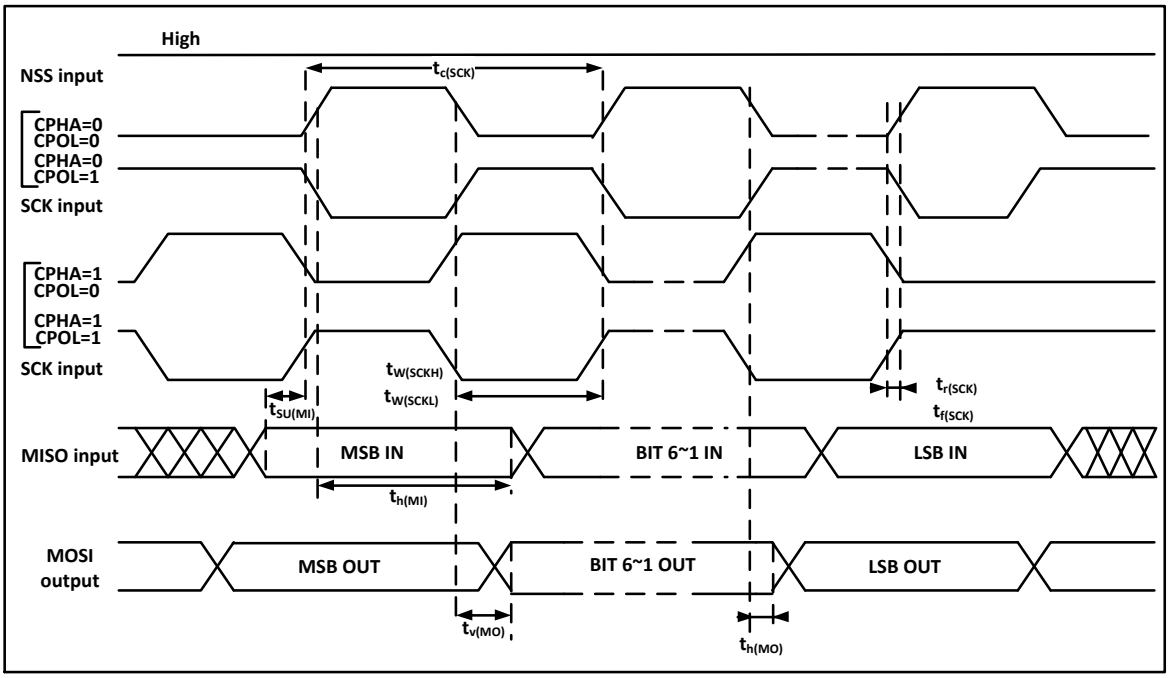



Figure 17. SPI Timing Diagram - Slave Mode and CPHA=1




(1) The measured points are done at CMOS levels:0.3$V_{DD}$ and 0.7$V_{DD}$。

Figure 18. SPI Timing Diagram - Master Mode(3)




(1) The measured points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$。

**USBD Interface Features**

Table 39.USBD DC Characteristics

| Symbol | Parameter | Conditions | Minimum Value (1) | Maximum Value (1) | Unit |
|---|---|---|---|---|---|
| Input levels | | | | | |
| $V_{DD}$ | USBD operating voltage (2) | | 3.0 (3) | 3.6 | V |
| $V_{DI}$ (4) | Differential input sensitivity | I（USBDP，USBDM） | 0.2 | | V |
| $V_{CM}$ (4) | Differential common mode threshold | Include $V_{DI}$ range | 0.8 | 2.5 | |
| $V_{SE}$ (4) | Single ended receiver threshold | | 1.3 | 2.0 | |
| Output levels | | | | | |
| $V_{OL}$ | Static output level low | $R_L$ of 1.5kΩto 3.6V (5) | | 0.3 | V |
| $V_{OH}$ | Static output level high | $R_L$ of 1.5kΩto $V_{SS}$ (5) | 2.8 | 3.6 | |

(1) All the voltages are measured from the local ground potential.

(2) In order to be compatible with USB2.0 full-speed electrical specification, USBDP (D +) pin must pass a 1.5 k Ω resistor connected to the voltage from 3.0 V to 3.6 V.

(3) The function of APM32F103xx can be guaranteed at 2.7V without the electrical characteristics of degradation in 2.7~ 3.0v voltage range.

(4) Guaranteed by comprehensive evaluation and is not tested in production.

(5) RL is the load connected on the USBD drivers.

Figure 19. USBD Timing: Definition of Data Signal Rise and Fall Times

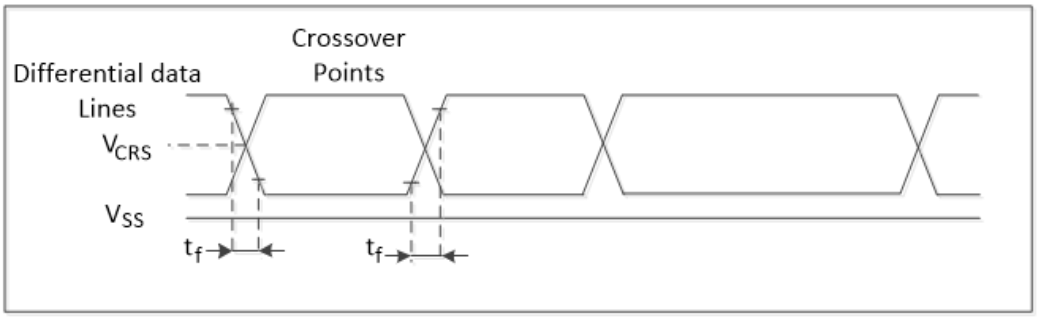



Table 40.USBD Full-speed Electrical Characteristics

| Symbol | Parameters | Conditions | Minimum Value | Maximum Value | Unit |
|---|---|---|---|---|---|
| $t_r$ | Rise Time | $C_L$ = 50pF | 4.6 | 9.3 | ns |
| $t_f$ | Fall Time | $C_L$ = 50pF | 5.2 | 10.9 | ns |
| $t_{rfm}$ | Rise&fall Times match | $t_r$ / $t_f$ | 71 | 97 | % |
| $V_{CRS}$ | Crossover voltage of output signal | | 1.60 | 2.17 | V |

## 5.3.11. 12-bit ADC Features

Table 41.ADC Features ($V_{DD}$= 2.4-3.6V，$T_A$=-40~105°C)

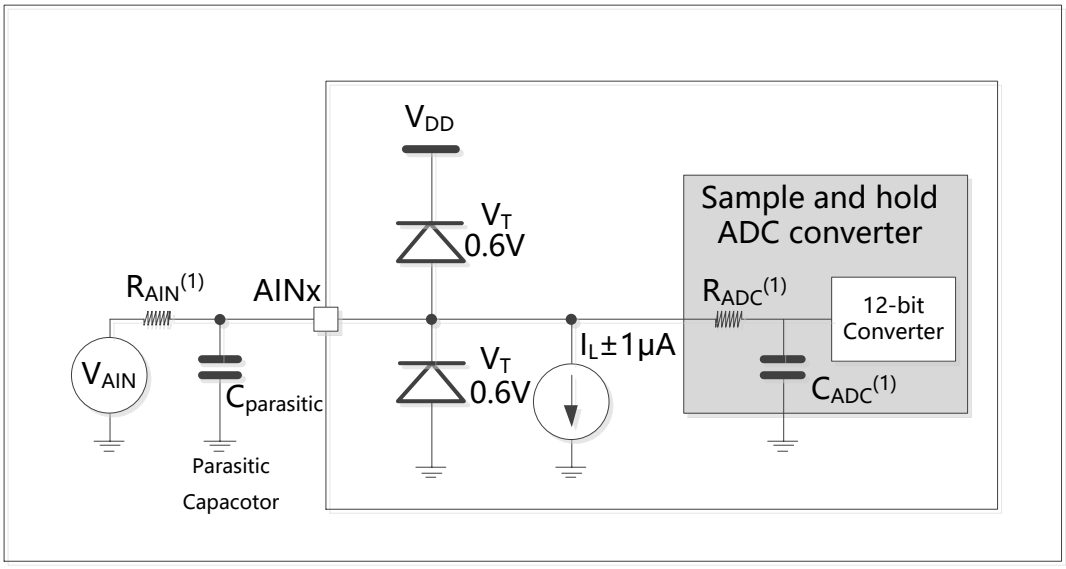
| Symbol | Parameters | Conditions | Minimum Value | Typical Value | Maximum Value | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Power supply | | 2.4 | | 3.6 | V |
| $V_{REF+}$ | Positive reference voltage | | 2.4 | | $V_{DDA}$ | V |
| $I_{VREF}$ | Current on $V_{REF+}$ input pin | | | 260 | 484 | μA |
| $f_{ADC}$ | ADC clock frequency | | 0.6 | | 14 | MHz |
| $f_S$ | Sampling rate | | 0.05 | | 1 | MHz |
| $V_{AIN}$ | Conversion voltage range | | 0 | | $V_{REF+}$ | V |

| Symbol | Parameters | Conditions | Minimum Value | Typical Value | Maximum Value | Unit |
|---|---|---|---|---|---|---|
| $t_{CAL}$ | Calibration Time | $f_{ADC}$ = 14MHz | | 5.9 | | μs |
| | | | | 83 | | $1/f_{ADC}$ |
| $R_{ADC}$ | Sampling resistor | | | 1 | | kΩ |
| $C_{ADC}$ | Sample and hold capacitor | | | 2 | | Pf |
| $t_S$ | Sampling Time | $f_{ADC}$ = 14MHz | 0.107 | | 17.1 | μs |
| | | | 1.5 | | 239.5 | $1/f_{ADC}$ |
| $t_{CONV}$ | Total conversion Time (includes sampling Time) | $f_{ADC}$ = 14MHz | 1 | | 18 | μs |
| | | | 14~252($t_S$ for sampling + 12.5 for successive approximation) | | | $1/f_{ADC}$ |

(1) Guaranteed by comprehensive evaluation and is not tested in production.

(2) $C_{parasitic}$ must be added to CAIN. It represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (3 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, $f_{ADC}$ should be reduced.

Figure 20. Typical application of ADC




The formula for calculating the maximum external input impedance is as follows：

Formula 1: formula of maximum $R_{AIN}$

$$R_{AIN} < \frac{T_S}{f_{ADC} \quad X \quad C_{ADC} \quad X \quad \ln(2^{N+2})} - R_{ADC}$$

$f_{ADC}$=14MHZ, $C_{ADC}$=12PF(Table 41), $R_{ADC}$=1kΩ(Table 41). Under the requirement of 0.25LSB sampling error accuracy, the relation between $T_S$ and $R_{AIN}$ is shown in the following table:

Table 42.Maximum $R_{AIN}$ at $f_{ADC}$=14MHz (1)

| TS（cycle） | $t_S$（μs） | Maximum $R_{AIN}$（kΩ） |
|---|---|---|
| 1.5 | 0.11 | 4.5 |
| 7.5 | 0.54 | 26.6 |
| 13.5 | 0.96 | 48.7 |
| 28.5 | 2.04 | 103.9 |
| 41.5 | 2.96 | 151.7 |
| 55.5 | 3.96 | 203.2 |

(1) Data is guaranteed from design and is not tested in production.

Table 43.ADC Accuracy

| Symbol | Parameter | Conditions | Typical value | Maximum value(3) | Unit |
|---|---|---|---|---|---|
| ET | Total error | $f_{PCLK2}$=56MHz, $f_{ADC}$=14MHz,$R_{AIN}$<10KΩ, $V_{DDA}$=2.4~3.6V,$T_A$=-40~105℃ Measurement was made after the ADC calibration | ±2.5 | ±5.5 | LSB |
| Eo | Offset error | | ±2.1 | ±3.5 | |
| EG | Gain error | | ±2.0 | ±4 | |
| ED | Differential linearity error | | ±1.5 | ±2.5 | |
| EL | Integral linearity error | | ±1.8 | ±3 | |

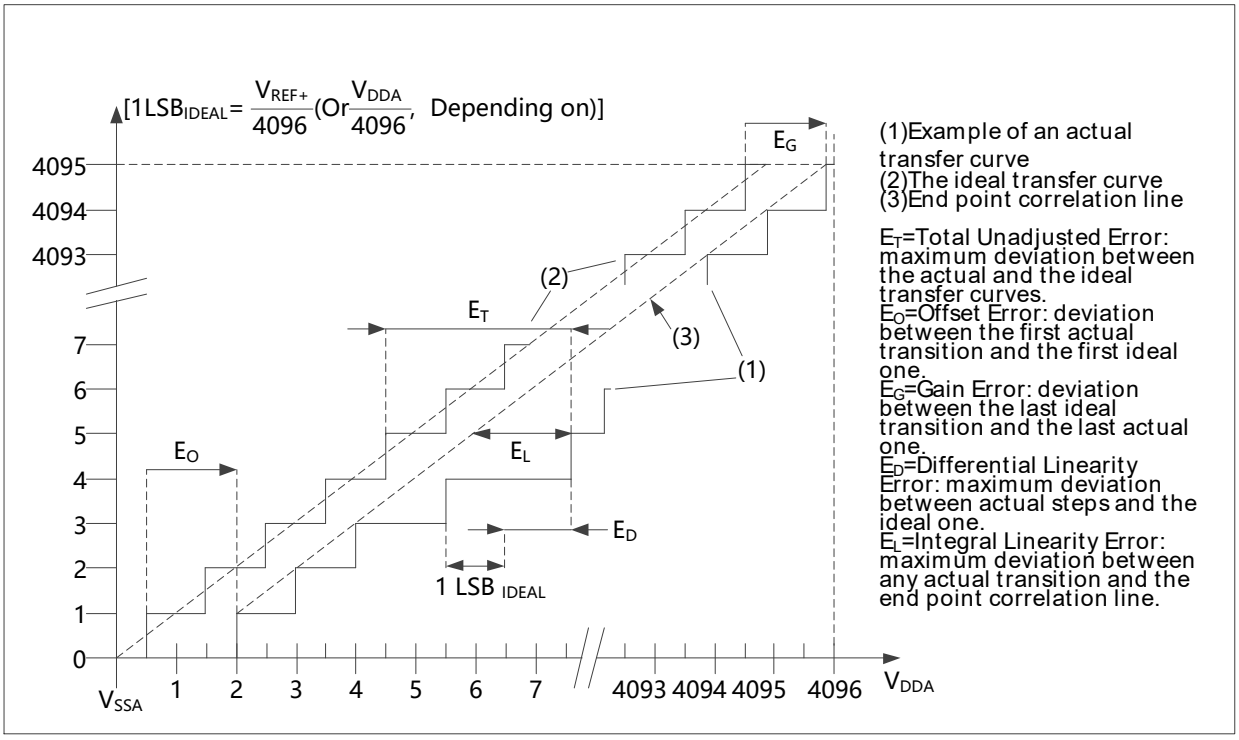
(1) DC accuracy value of ADC is measured after internal calibration

(2) ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.

Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $I_{INJ(PIN)}$ in Section 5.3.32 does not affect the ADC accuracy.

(3) Guaranteed by comprehensive evaluation and is not tested in production.

Figure 21. ADC Accuracy Characteristics




## 5.3.12. Temperature Sensor Features

Table 44.Temperature Sensor Features

| Symbol | Parameters | Minimum Value | Typical Value | Maximum Value | Unit |
|---|---|---|---|---|---|
| Avg_Slope(1) | Average slope ($V_{DD}$ = 3.3V, $T_A$ = -40~105°C) | 4.1 | 4.2 | 4.5 | mV/ºC |
| $V_{25}$ | Voltage at 25ºC ($V_{DD}$ =2.4-3.6V) | 1.38 | 1.41 | 1.44 | V |
| $t_{START}$(2) | Setup Time | 4 | | 10 | μs |
| $T_{S\_temp}$(2) (3) | ADC sampling Time when reading the temperature | | | 17.1 | μs |

(1) Data is guaranteed by analysis on features, and is not tested in production.

(2) Data is guaranteed from design, and is not tested in production.

(3) The shortest sampling Time can be determined by the application through multiple iterations.

## 5.3.13. EMC Features

Sensitivity tests are sampled for testing during a comprehensive evaluation on the product.

**Electromagnetic Sensitivity (EMS)**

When running a simple application (controlling 2 LEDs flashing through the I/O port), the test sample is spurious electromagnetic interference until an error occurs, and LED flashing

indicates an error. The test complies with IEC61000-4-4 standard.

Table 45.EMS Features

| Symbol | Parameters | Conditions | Level |
|---|---|---|---|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance. | $V_{DD}$ = 3.3V，$T_A$ = +25 °C，$f_{HCLK}$ = 72MHz, complies with IEC 61000-4-2 | 2B |
| $V_{EFTB}$ | Fast transit voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance. | $V_{DD}$ = 3.3V，$T_A$ = +25 °C，$f_{HCLK}$ = 72MHz, complies with IEC 61000-4-4 | 2B |

**Electromagnetic Interference (EMI)**

Monitor the electromagnetic field emitted by the chip while running a simple application (flashing 2 LEDs through the I/O port). This emission test complies with the SAE J1752/3 standard, which specifies the load on the test board and pins.

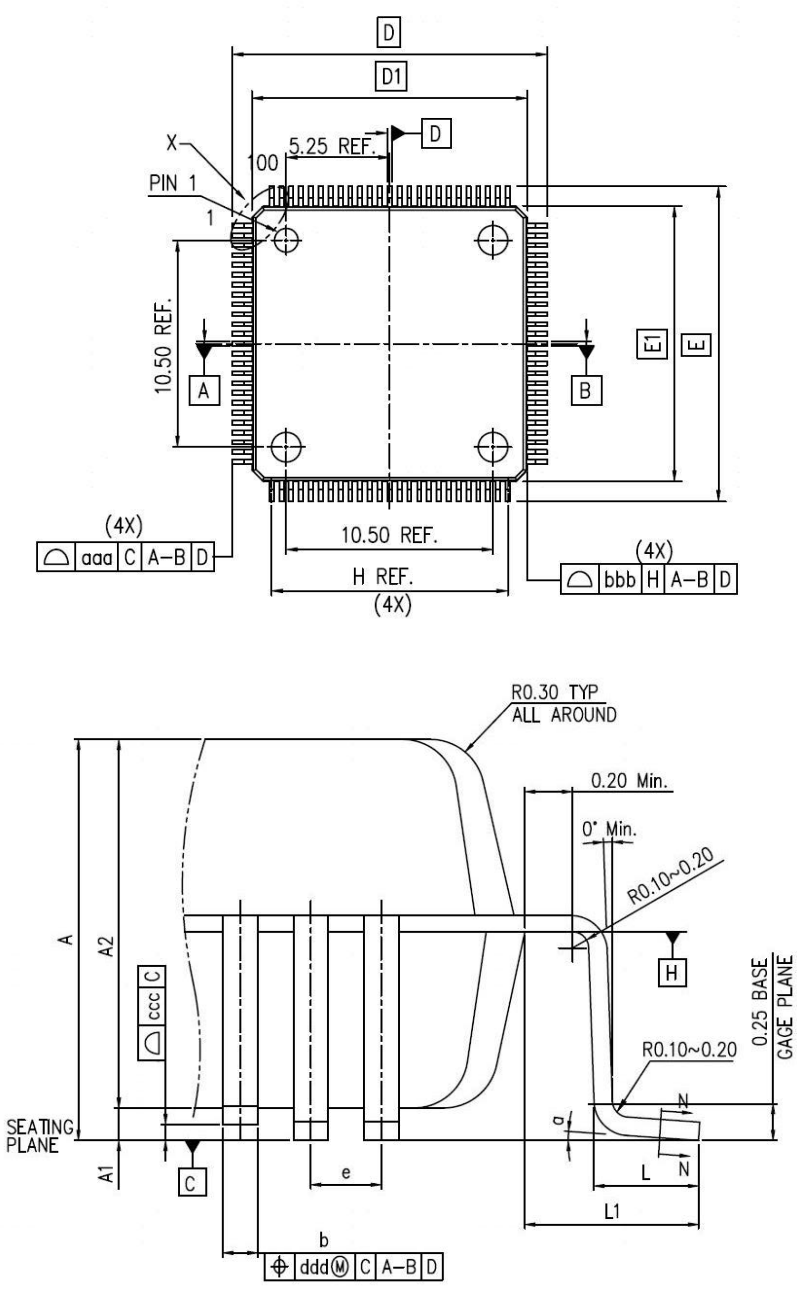
Table 46.EMI Features

| Symbol | Parameters | Conditions | Detection frequency band | Maximum value ($f_{HSECLK}$/$f_{HCMU}$) | | Unit |
|---|---|---|---|---|---|---|
| | | | | 8/36MHz | 8/96MHz | |
| SEMI | Peak | $V_{DD}$ = 3.3V，$T_A$ = +25 °C, LQFP100 package | 30-230MHz | PASS | PASS | dBμV |
| | | | 130MHz-1GHz | PASS | PASS | |

# 6. Packaging Information

## 6.1. LQFP100 Package Diagram

Figure 22. LQFP100 Package Diagram




(1) Drawing is not to scale.

(2) The inside of the pad on the back is not connected to $V_{SS}$ or $V_{DD}$.

(3) There is a pad on the bottom of the QPN package that should be soldered to the PCB.

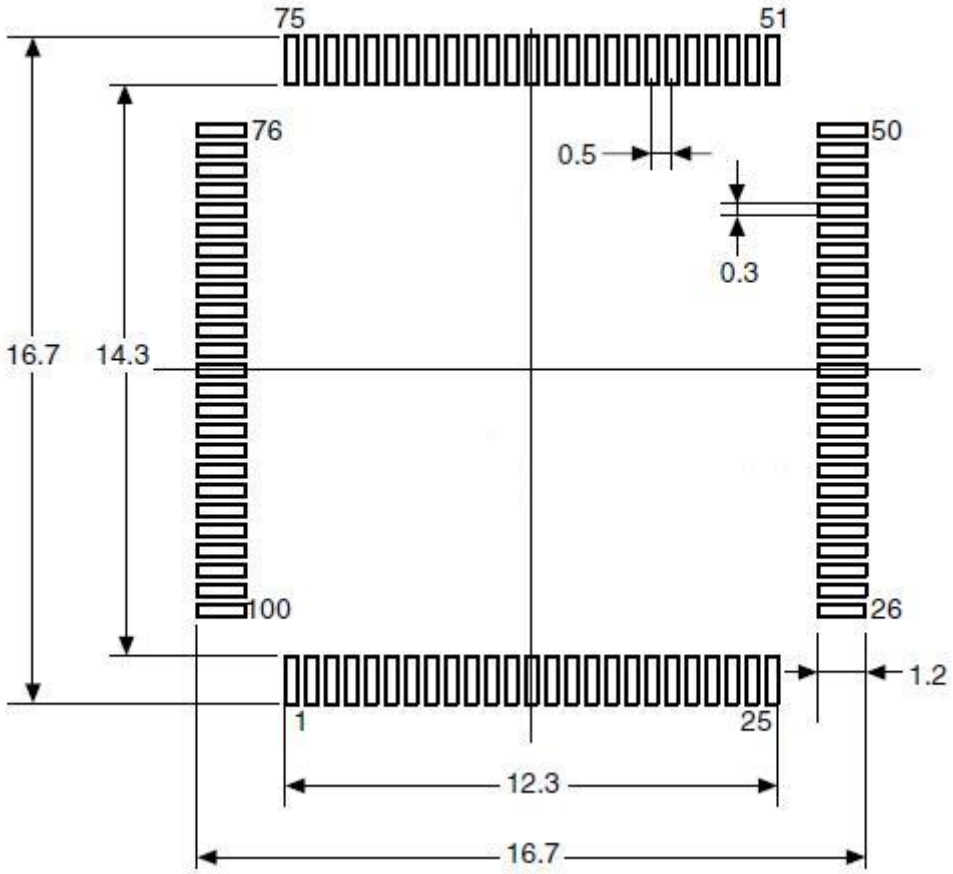
(4) All pins should be soldered to the PCB.

Table 47.LQFP100 Package Data

| DIMENSION LIST(FOOTPRINT: 2.00) | | | |
|---|---|---|---|
| **S/N** | **SYM** | **DIMENDIONS** | **REMARKS** |
| 1 | A | MAX. 1.60 | OVERALL HEIGHT |
| 2 | A1 | 0.1±0.05 | STANDOFF |
| 3 | A2 | 1.40±0.05 | PKG THICKNESS |
| 4 | D | 16.00±0.20 | LEAD TIP TO TIP |
| 5 | D1 | 14.00±0.10 | PKG LENGTH |
| 6 | E | 16.00±0.20 | LEAD TIP TO TIP |
| 7 | E1 | 14.00±0.10 | PKG WDTH |
| 8 | L | 0.60±0.15 | FOOT LENGTH |
| 9 | L1 | 1.00 REF | LEAD LENGTH |
| 10 | T | 0.15 | LEAD THICKNESS |
| 11 | T1 | 0.127±0.03 | LEAD BASE METAL THICKNESS |
| 12 | a | 0°~7° | FOOT ANGLE |
| 13 | b | 0.22±0.02 | LEAD WIDTH |
| 14 | b1 | 0.20±0.03 | LEAD BASE METAL WIDTH |
| 15 | e | 0.50 BASE | LEAD PITCH |
| 16 | H(REF.) | (12.00) | CUM. LEAD PITCH |
| 17 | aaa | 0.2 | PROFILE OF LEAD TIPS |
| 18 | bbb | 0.2 | PROFILE OF MOLD SURFACE |
| 19 | ccc | 0.08 | FOOT COPLANARITY |
| 20 | ddd | 0.08 | FOOT POSITION |

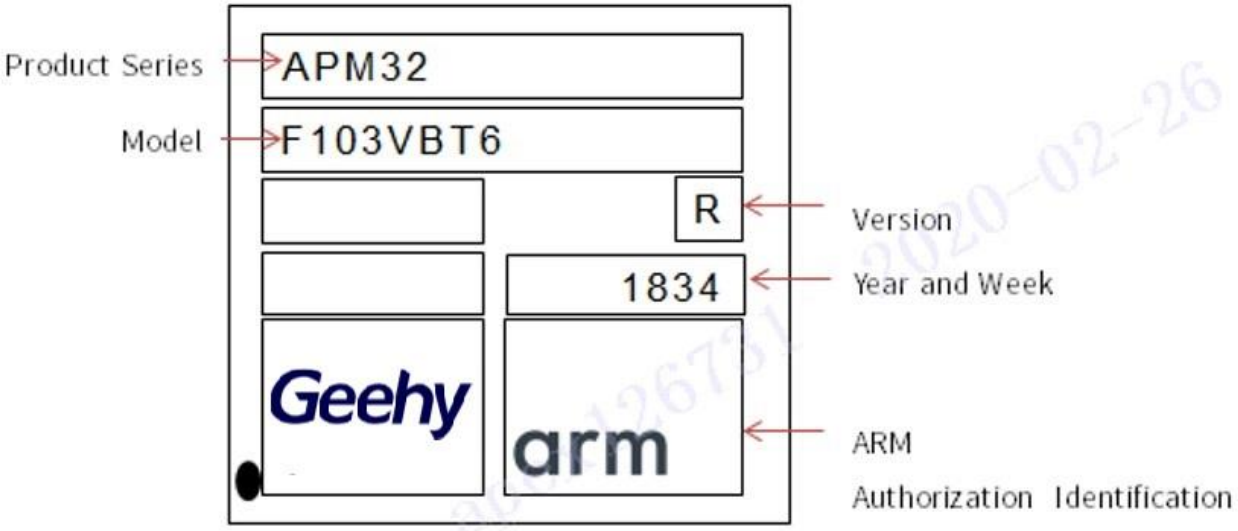
(1) Dimensions in millimeters

Figure 23. LQFP100-100 pins,14x14mm welding Layout proposal



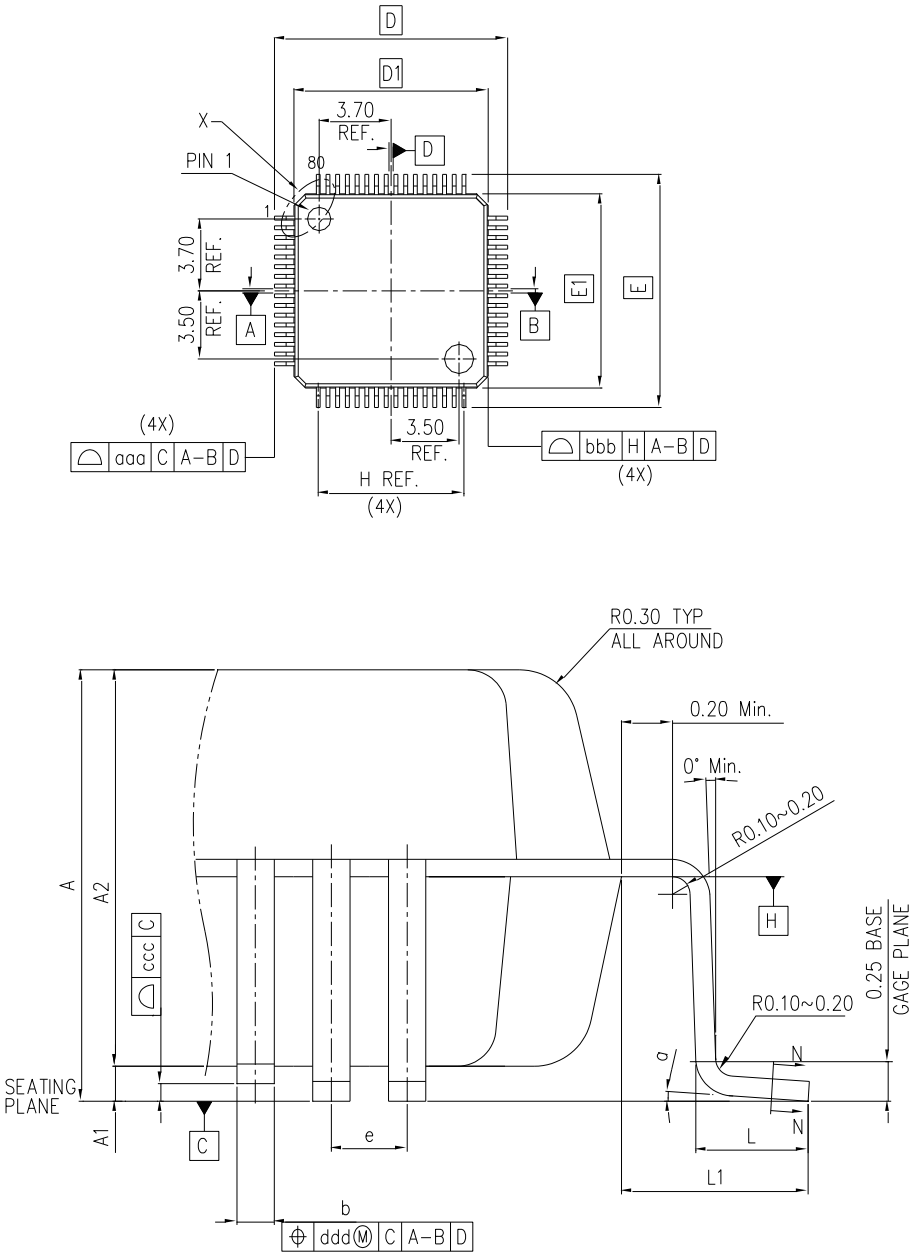

1.Dimensions in millimeters。

Figure 24. LQFP100-100 pin,14x14mm package identification diagram



## 6.2. LQFP64 Package Diagram

Figure 25. LQFP64 Package Diagram




(1) Drawing is not to scale.

(2) The inside of the pad on the back is not connected to VSS or VDD.

(3) There is a pad on the bottom of the QPN package that should be soldered to the PCB.

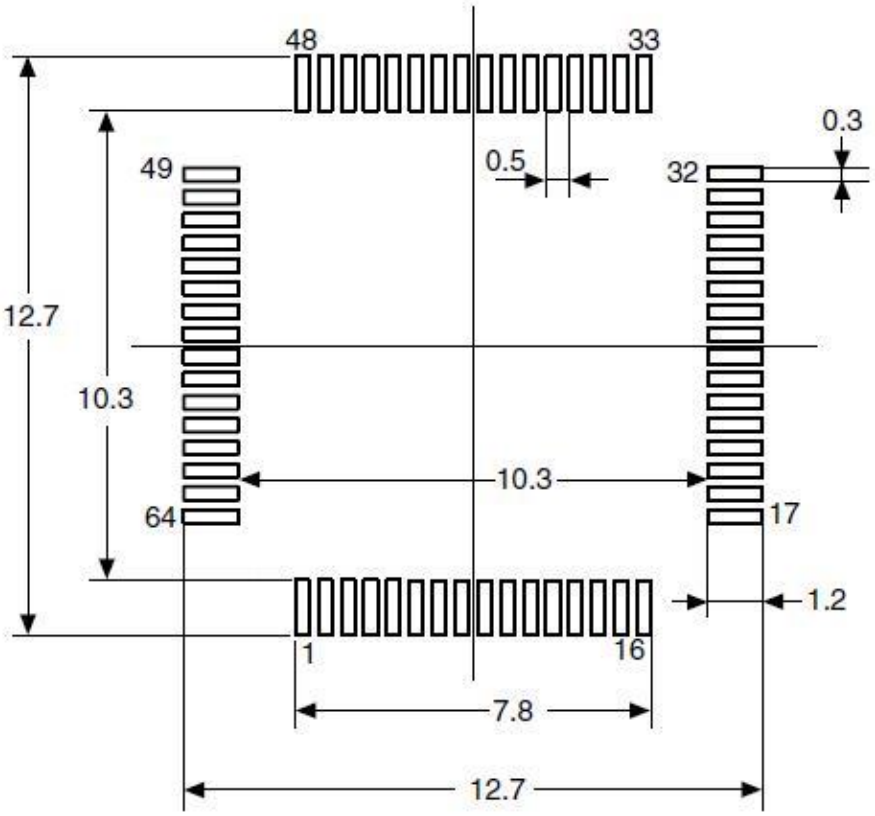
(4) All pins should be soldered to the PCB.

Table 48.LQFP64 Package Data

| DIMENSION LIST(FOOTPRINT: 2.00) | | | |
|---|---|---|---|
| S/N | SYM | DIMENDIONS | REMARKS |
| 1 | A | MAX. 1.600 | OVERALL HEIGHT |
| 2 | A1 | 0.100±0.050 | STANDOFF |
| 3 | A2 | 1.400±0.050 | PKG THICKNESS |
| 4 | D | 12.000±0.200 | LEAD TIP TO TIP |
| 5 | D1 | 10.000±0.100 | PKG LENGTH |
| 6 | E | 12.000±0.200 | LEAD TIP TO TIP |
| 7 | E1 | 10.000±0.100 | PKG WDTH |
| 8 | L | 0.600±0.150 | FOOT LENGTH |
| 9 | L1 | 1.000 REF | LEAD LENGTH |
| 10 | T | 0.150 | LEAD THICKNESS |
| 11 | T1 | 0.127±0.030 | LEAD BASE METAL THICKNESS |
| 12 | a | 0°~7° | FOOT ANGLE |
| 13 | b | 0.220±0.050 | LEAD WIDTH |
| 14 | b1 | 0.200±0.030 | LEAD BASE METAL WIDTH |
| 15 | e | 0.500 BASE | LEAD PITCH |
| 16 | H(REF.) | (7.500) | CUM. LEAD PITCH |
| 17 | aaa | 0.2 | PROFILE OF LEAD TIPS |
| 18 | bbb | 0.2 | PROFILE OF MOLD SURFACE |
| 19 | ccc | 0.08 | FOOT COPLANARITY |
| 20 | ddd | 0.08 | FOOT POSITION |

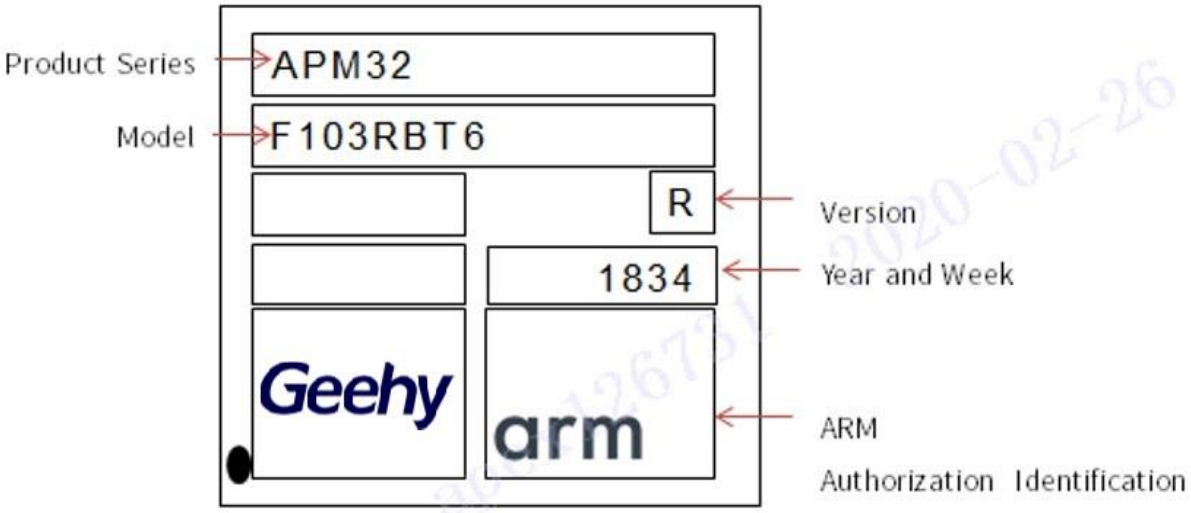
(1) Dimensions in millimeters。

Figure 26. LQFP64-64 pin,10x10mm welding Layout proposal



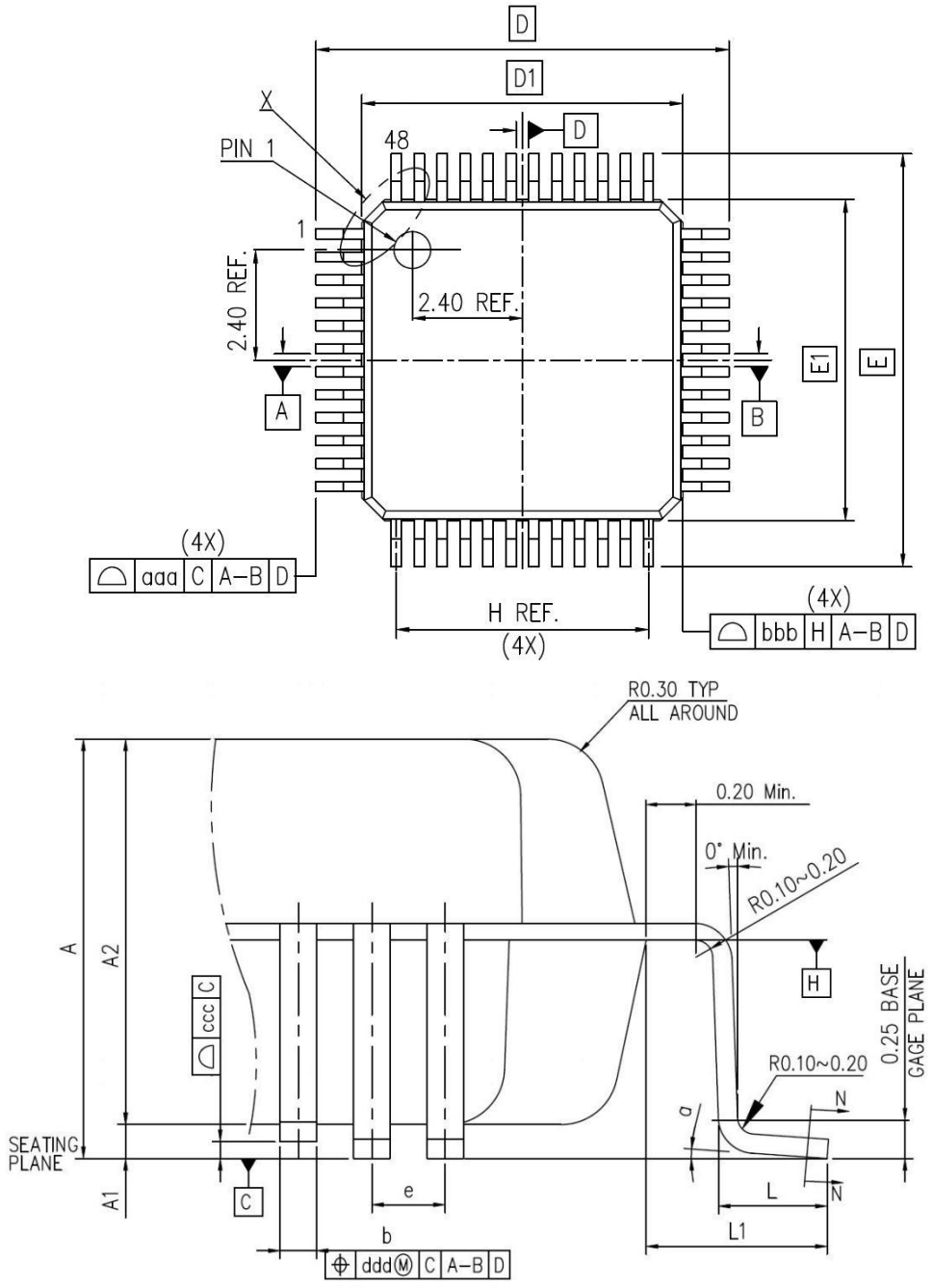

(1) Dimensions in millimeters。

Figure 27. LQFP64-64 pin,10x10mm package identification diagram



## 6.3. LQFP48 Package Diagram

Figure 28. LQFP48 Package Diagram




(1) Drawing is not to scale.

(2) The inside of the pad on the back is not connected to VSS or VDD.

(3) There is a pad on the bottom of the QPN package that should be soldered to the PCB.

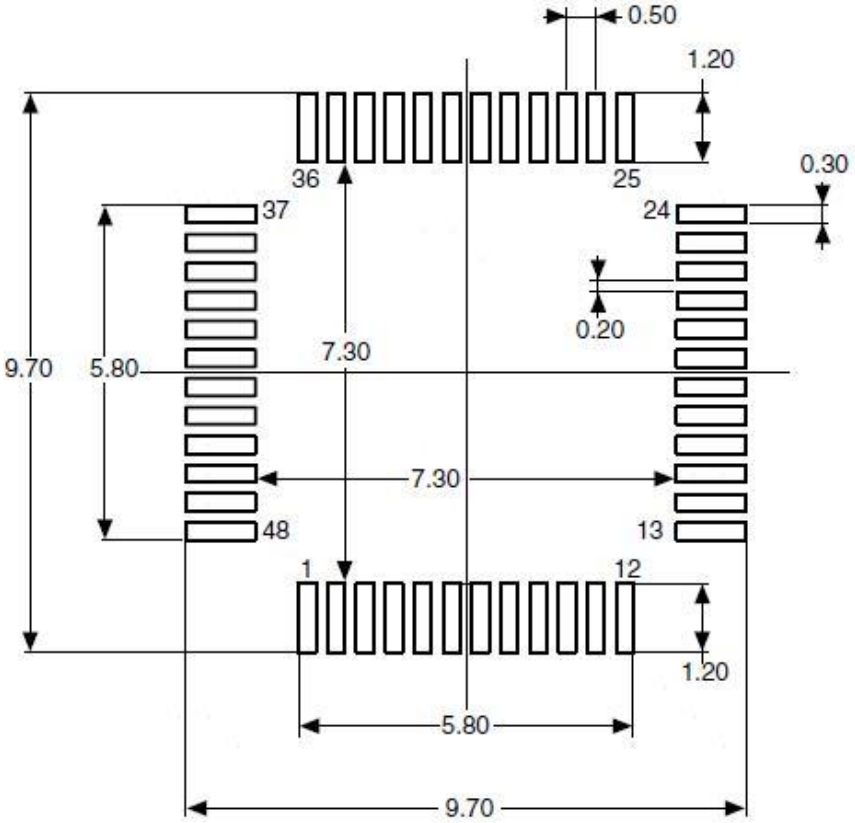
(4) All pins should be soldered to the PCB.

Table 49.LQFP Package Data

| DIMENSION LIST(FOOTPRINT: 2.00) | | | |
|---|---|---|---|
| **S/N** | **SYM** | **DIMENDIONS** | **REMARKS** |
| 1 | A | MAX. 1.60 | OVERALL HEIGHT |
| 2 | A1 | 0.1±0.05 | STANDOFF |
| 3 | A2 | 1.40±0.05 | PKG THICKNESS |
| 4 | D | 9.00±0.20 | LEAD TIP TO TIP |
| 5 | D1 | 7.00±0.10 | PKG LENGTH |
| 6 | E | 9.00±0.20 | LEAD TIP TO TIP |
| 7 | E1 | 7.00±0.10 | PKG WDTH |
| 8 | L | 0.60±0.15 | FOOT LENGTH |
| 9 | L1 | 1.00 REF | LEAD LENGTH |
| 10 | T | 0.15 | LEAD THICKNESS |
| 11 | T1 | 0.127±0.03 | LEAD BASE METAL THICKNESS |
| 12 | a | 0°~7° | FOOT ANGLE |
| 13 | b | 0.22±0.02 | LEAD WIDTH |
| 14 | b1 | 0.20±0.03 | LEAD BASE METAL WIDTH |
| 15 | e | 0.50 BASE | LEAD PITCH |
| 16 | H(REF.) | (5.50) | CUM. LEAD PITCH |
| 17 | aaa | 0.2 | PROFILE OF LEAD TIPS |
| 18 | bbb | 0.2 | PROFILE OF MOLD SURFACE |
| 19 | ccc | 0.08 | FOOT COPLANARITY |
| 20 | ddd | 0.08 | FOOT POSITION |

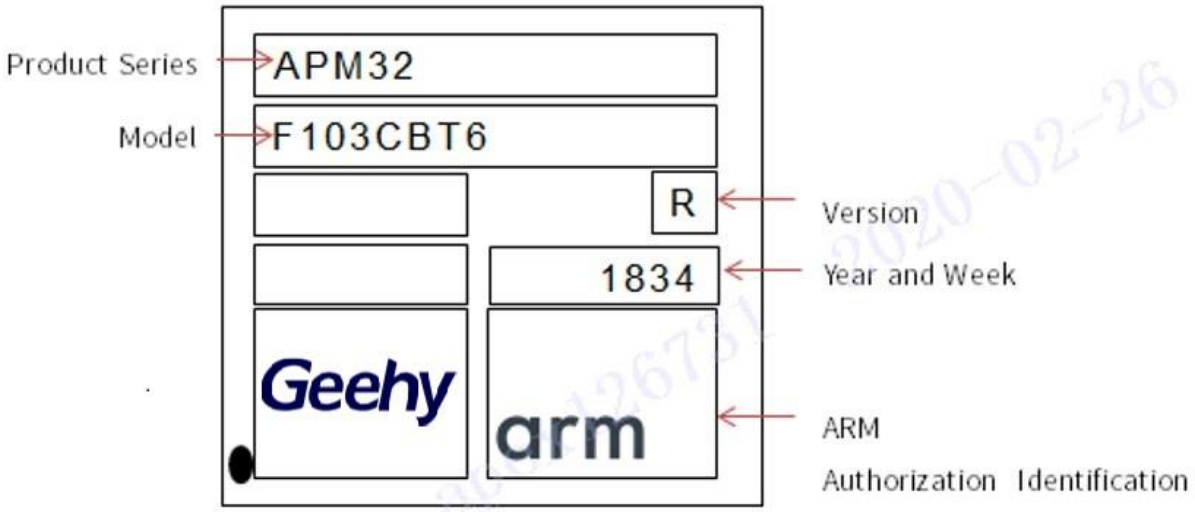
(1) dimensions in millimeters。

Figure 29. LQFP48-48 pin,7x7mm welding Layout proposal



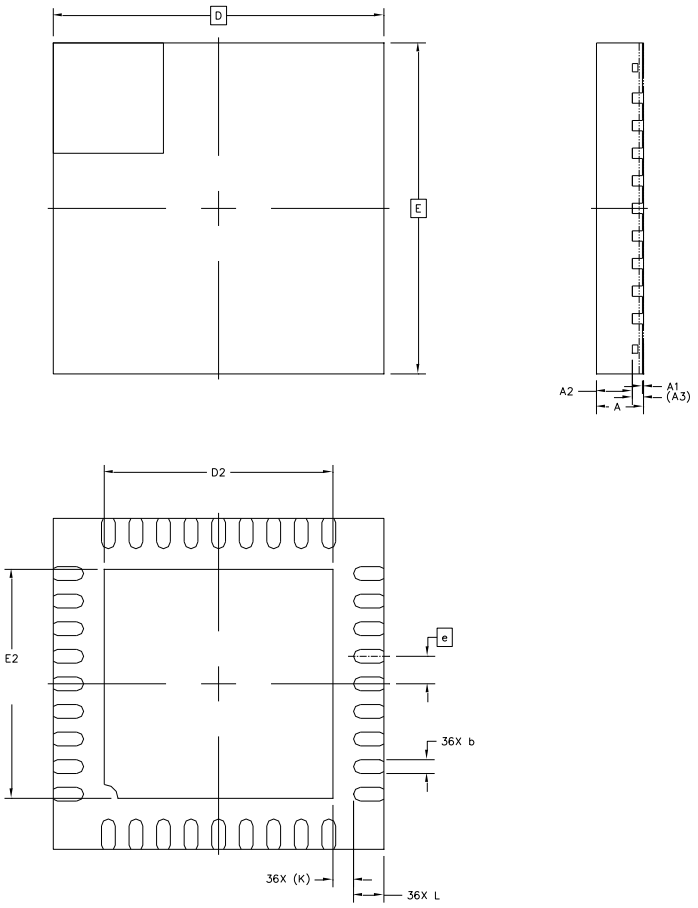

(1) Dimensions in millimeters。

Figure 30. LQFP48-48 pin,7x7mm identification diagram



## 6.4. QFN36 Package Diagram

Figure 31. QFN36 Package Diagram




(1) Drawing is not to scale.

(2) The inside of the pad on the back is not connected to $V_{SS}$ or $V_{DD}$.

(3) There is a pad on the bottom of the QPN package that should be soldered to the PCB.

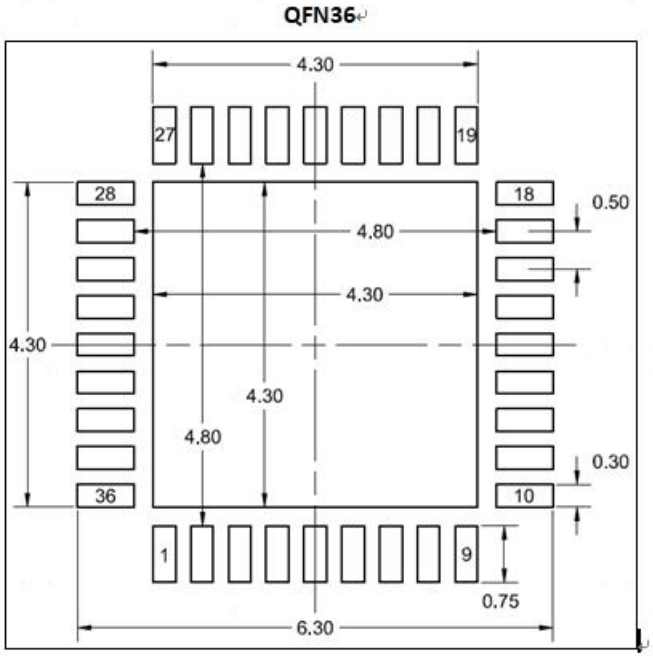
(4) All pins should be soldered to the PCB.

Table 50.QFN36 Package Data

| | | SYMBOL | MIN | NOD | MAX |
|---|---|---|---|---|---|
| TOTAL THCKNESS | | A | 0.8 | 0.85 | 0.9 |
| STANO OFF | | A1 | 0 | 0.02 | 0.05 |
| MOLO THCKNESS | | A2 | --- | 0.65 | --- |
| L/F THCKNESS | | A3 | 0.203REF | | |
| LEAD WIDTH | | b | 0.2 | 0.25 | 0.3 |
| BOOY SIZE | X | D | 6 BSC | | |
| | Y | E | 6 BSC | | |
| LEAD PITCH | | e | 0.5 BSC | | |
| EP SIZE | X | D2 | 4.05 | 4.15 | 4.25 |
| | Y | E2 | 4.05 | 4.15 | 4.25 |
| LEAD LENGTH | | L | 0.45 | 0.55 | 0.65 |
| LEAD TIP TO EXPOSE PAD EDGE | | k | 0.375 REF | | |
| PACKAGE EOGE TOLERANCE | | aaa | 0.1 | | |
| MOLD FLATNESS | | ccc | 0.1 | | |
| COPLANARITY | | eee | 0.08 | | |
| LEAD OFFSET | | bbb | 0.1 | | |
| EXPOSED PAD OFFSET | | fff | 0.1 | | |

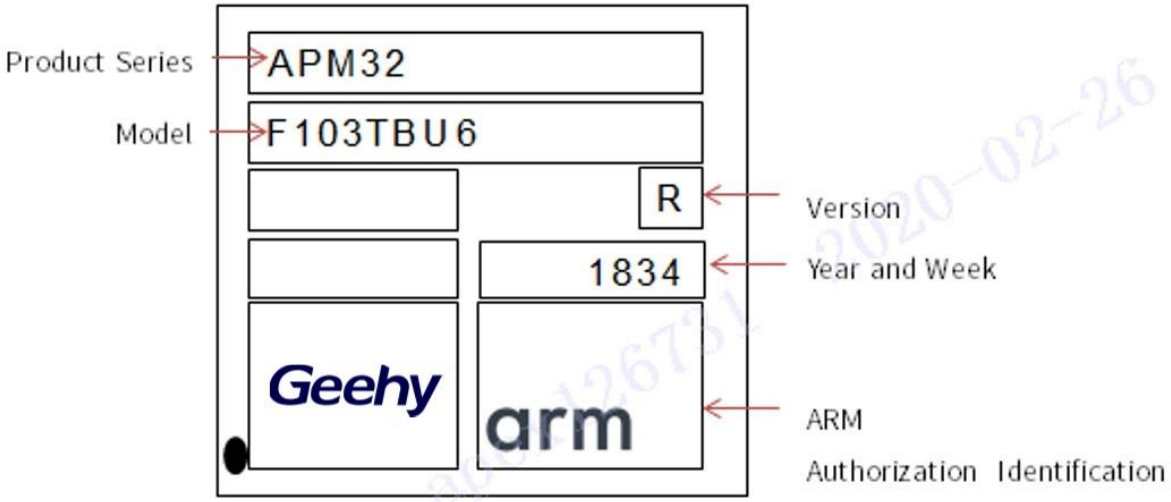
(1) dimensions in millimeters。

Figure 32. QFN36 pin, 6 x 6mm Welding Layout Proposal




(1) Dimensions in millimeters。

Figure 33. QFN36 pin, 6x6mm identification diagram



# 7. Ordering Information

Example: APM32 F 103 C B T 6 XXX

Device family

APM32 = ARM-based 32-bit microcontroller

**Product type**

F = general-purpose

**Device subfamily**

103 = performance line

**Pin count**

T = 36 pins
C = 48 pins
R = 64 pins
V = 100 pins

**Flash memory size**

B = 128 Kbytes of Flash memory

**Package**

T=LQFP
U=QFN

**Temperature range**

6 = Industrial temperature range, -40 to 85°C
7 = Industrial temperature range, -40 to 105°C

**Options**

xxx= programmed parts
R = tape and real
Blank = tray

Table 51.Ordering Information Table

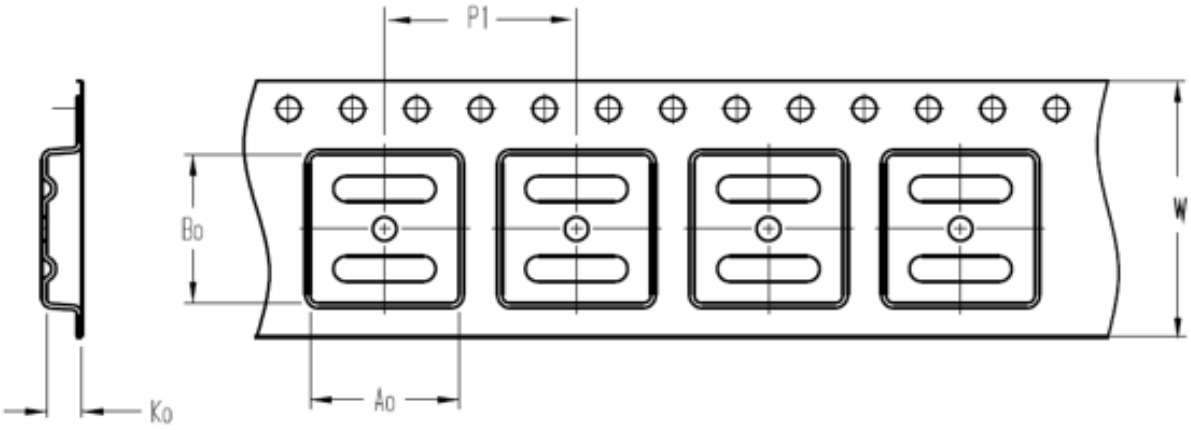
| Oder No. | FLASH(KB) | SRAM(KB) | Package | SPQ | Temperature range |
|---|---|---|---|---|---|
| APM32F103TBU6 | 128 | 20 | QFN36 | 4900 | industrial level -40℃~85℃ |
| APM32F103CBT6 | 128 | 20 | LQFP48 | 2500 | industrial level -40℃~85℃ |
| APM32F103RBT6 | 128 | 20 | LQFP64 | 1600 | industrial level -40℃~85℃ |
| APM32F103VBT6 | 128 | 20 | LQFP100 | 900 | industrial level -40℃~85℃ |
| APM32F102CBT6 | 128 | 20 | LQFP48 | 2500 | industrial level -40℃~85℃ |
| APM32F102RBT6 | 128 | 20 | LQFP64 | 1600 | industrial level -40℃~85℃ |
| APM32F101TBU6 | 128 | 20 | QFN36 | 4900 | industrial level -40℃~85℃ |
| APM32F101CBT6 | 128 | 20 | LQFP48 | 2500 | industrial level -40℃~85℃ |
| APM32F101RBT6 | 128 | 20 | LQFP64 | 1600 | industrial level -40℃~85℃ |
| APM32F101VBT6 | 128 | 20 | LQFP100 | 900 | industrial level -40℃~85℃ |
| APM32F103TBU6-R | 128 | 20 | QFN36 | 2500 | industrial level -40℃~85℃ |
| APM32F103CBT6-R | 128 | 20 | LQFP48 | 2000 | industrial level -40℃~85℃ |
| APM32F103RBT6-R | 128 | 20 | LQFP64 | 1000 | industrial level -40℃~85℃ |
| APM32F102CBT6-R | 128 | 20 | LQFP48 | 2000 | industrial level -40℃~85℃ |
| APM32F102RBT6-R | 128 | 20 | LQFP64 | 1000 | industrial level -40℃~85℃ |
| APM32F101TBU6-R | 128 | 20 | QFN36 | 2500 | industrial level -40℃~85℃ |
| APM32F101CBT6-R | 128 | 20 | LQFP48 | 2000 | industrial level -40℃~85℃ |
| APM32F101RBT6-R | 128 | 20 | LQFP64 | 1000 | industrial level -40℃~85℃ |

note：SPQ：The minimum number of packages.

# 8. Package Information

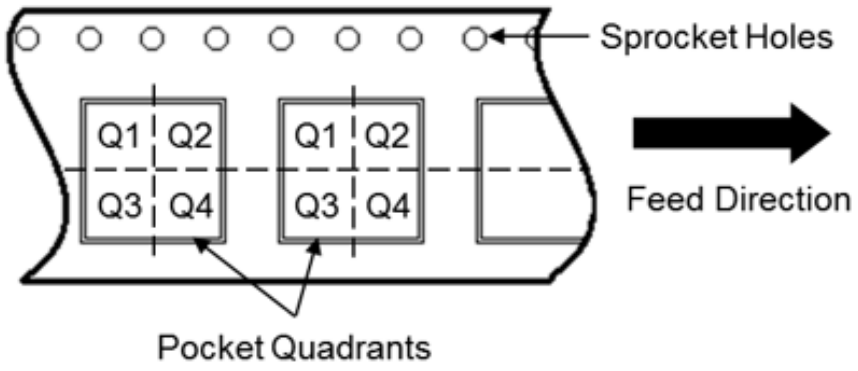
Figure 34. Strip Package Specification Diagram

**Tape Dimensions**

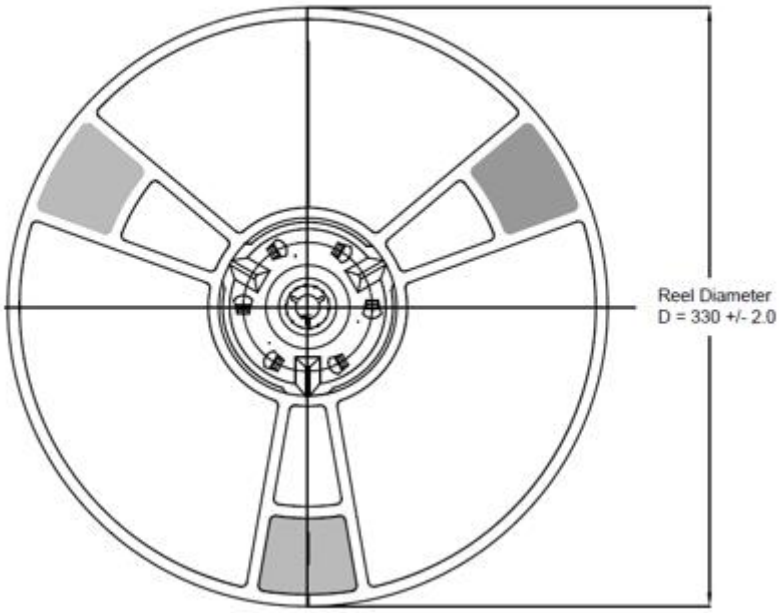



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**Quadrant Assignments For PIN1 Orientation In Tape**



**Reel Dimensions**

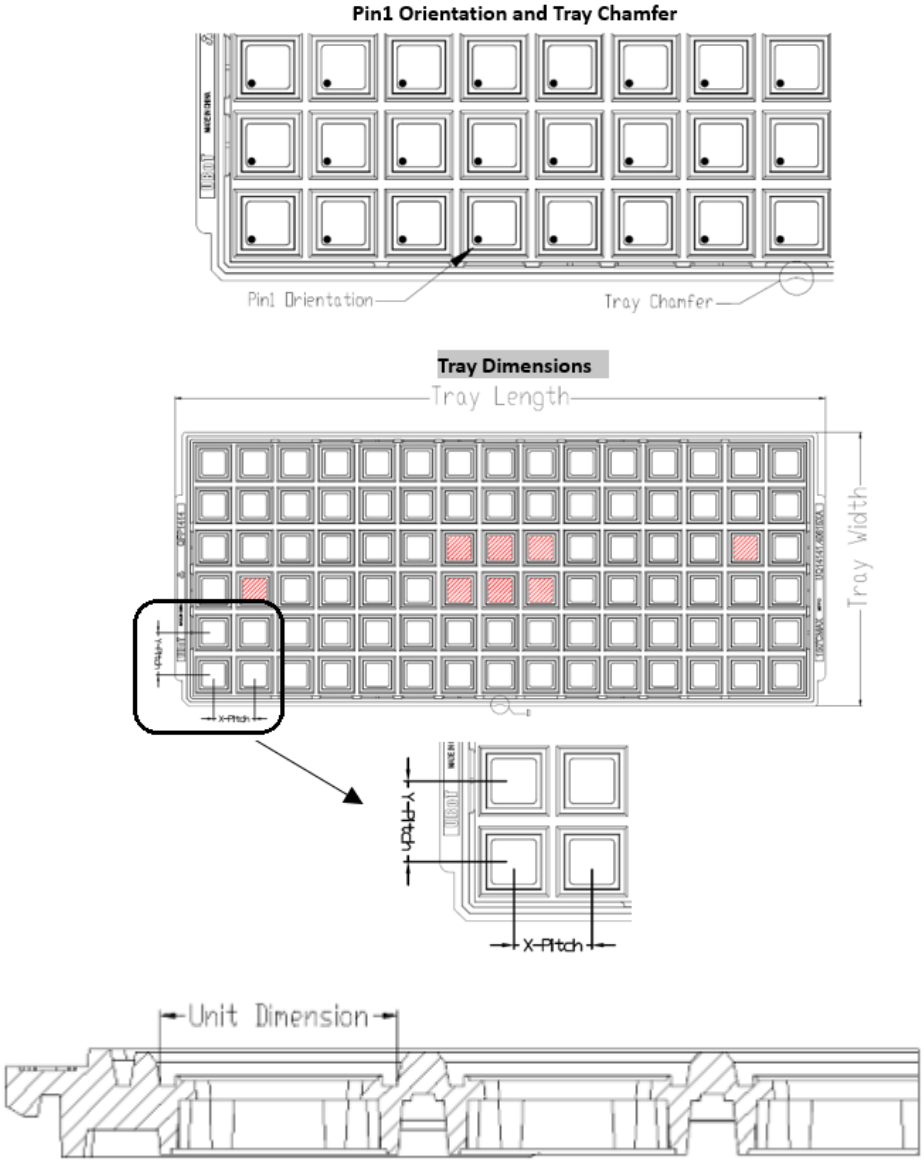



All pictures are only for reference, appearance depends on products

Table 52.Strip Package Parameters Specification

| Device | Package Type | Pins | SPQ | Reel Diameter (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|
| APM32F103RBT6 | LQFP | 64 | 1000 | 330 | 12.35 | 12.35 | 2.2 | 16 | 24 | Q1 |
| APM32F102RBT6 | LQFP | 64 | 1000 | 330 | 12.35 | 12.35 | 2.2 | 16 | 24 | Q1 |
| APM32F101RBT6 | LQFP | 64 | 1000 | 330 | 12.35 | 12.35 | 2.2 | 16 | 24 | Q1 |
| APM32F103CBT6 | LQFP | 48 | 2000 | 330 | 9.3 | 9.3 | 2.2 | 12 | 16 | Q1 |
| APM32F102CBT6 | LQFP | 48 | 2000 | 330 | 9.3 | 9.3 | 2.2 | 12 | 16 | Q1 |
| APM32F101CBT6 | LQFP | 48 | 2000 | 330 | 9.3 | 9.3 | 2.2 | 12 | 16 | Q1 |
| APM32F103TBU6 | QFN | 36 | 2500 | 330 | 6.4 | 6.4 | 1.4 | 8 | 16 | Q1 |
| APM32F101TBU6 | QFN | 36 | 2500 | 330 | 6.4 | 6.4 | 1.4 | 8 | 16 | Q1 |

Figure 35. Tray Package Diagram




All the pictures are only for reference, appearance depends on products

Table 53.Tray Package Parameters Specification

| Device | Package Type | Pins | SPQ | X-Dimension | Y-Dimension | X-Pitch | Y-Pitch | Tray Length | Tray Width |
|---|---|---|---|---|---|---|---|---|---|
| | | | | (mm) | (mm) | (mm) | (mm) | (mm) | (mm) |
| APM32F103VBT6 | LQFP | 100 | 900 | 16.6 | 16.6 | 20.3 | 21 | 322.6 | 135.9 |
| APM32F101VBT6 | LQFP | 100 | 900 | 16.6 | 16.6 | 20.3 | 21 | 322.6 | 135.9 |
| APM32F103RBT6 | LQFP | 64 | 1600 | 12.3 | 12.3 | 15.2 | 15.7 | 322.6 | 135.9 |
| APM32F102RBT6 | LQFP | 64 | 1600 | 12.3 | 12.3 | 15.2 | 15.7 | 322.6 | 135.9 |
| APM32F101RBT6 | LQFP | 64 | 1600 | 12.3 | 12.3 | 15.2 | 15.7 | 322.6 | 135.9 |
| APM32F103CBT6 | LQFP | 48 | 2500 | 9.7 | 9.7 | 12.2 | 12.6 | 322.6 | 135.9 |

| Device | Package Type | Pins | SPQ | X-Dimension | Y-Dimension | X-Pitch | Y-Pitch | Tray Length | Tray Width |
|---|---|---|---|---|---|---|---|---|---|
| | | | | (mm) | (mm) | (mm) | (mm) | (mm) | (mm) |
| APM32F102CBT6 | LQFP | 48 | 2500 | 9.7 | 9.7 | 12.2 | 12.6 | 322.6 | 135.9 |
| APM32F101CBT6 | LQFP | 48 | 2500 | 9.7 | 9.7 | 12.2 | 12.6 | 322.6 | 135.9 |
| APM32F103TBU6 | QFN | 36 | 4900 | 6.2 | 6.2 | 8.8 | 9.2 | 322.6 | 135.9 |
| APM32F101TBU6 | QFN | 36 | 4900 | 6.2 | 6.2 | 8.8 | 9.2 | 322.6 | 135.9 |

# 9. Commonly Used Function Module Denomination

Table 54.Commonly Used Function Module Denomination

| Module Function | short title |
|---|---|
| Reset management unit | RMU |
| Clock management unit | CMU |
| Reset and Clock management unit | RCM |
| External Interrupt | EINT |
| General Purpose IO | GPIO |
| Alternate Function IO | AFIO |
| Wakeup controller | WUPT |
| Buzzer | BUZZER |
| Independent watchdog timer | IWDT |
| Window watchdog timer | WWDT |
| Timer | TMR |
| CRC Controller | CRC |
| Power management unit | PMU |
| The banked register | BAKPR |
| DMA Controller | DMA |
| analog-digital converter | ADC |
| digital-analog converter | DAC |
| Real-time clock | RTC |
| External storage controller | EMMC |
| SDIO Interface | SDIO |
| USB Device Controller | USBD |
| Controller Local Area Network | CAN |
| USBD OTG | OTG |
| Ethernet | ETH |
| I2C Interface | I2C |
| Serial Peripheral Interface | SPI |
| Universal Asynchronous Receiver / Transmitter | UART |
| Universal Asynchronous/Synchronous Receiver / Transmitter | USART |
| Flash memory interface control unit | FMC |

# 10. Reversion History

Table 55.Document Reversion History

| Date | Version | Changes |
|---|---|---|
| 2/14/2019 | 1.0.0 | Initial release |
| 2/26/2019 | 1.0.1 | Add the notes in Table 8 |
| 5/6/2019 | 1.0.2 | Voltage was changed from 1.8V to 1.6V |
| 1/3/2020 | 1.0.3 | Added electrical characteristics and commonly used function module denomination, and modified the cover |
| 1/24/2020 | 1.0.4 | Extracted section 5.3 from section 5.2 |
| 3/4/2020 | 1.0.5 | Generated section 3.14.2 |
| 6/22/2020 | 1.1.0 | Adjust product characteristics, system block diagram, clock tree, storage map, power supply scheme |
| 7/6/2020 | 1.1.1 | Modified the directory format |
| 9/9/2020 | 1.2 | (1) to modify the chapter 7 "order information naming specification", "order information list" in the table to add "minimum packing number", "ordering code"<br>(2) modifying the document font format |
| 12/22/2020 | 1.2 | (1) Change Note 7 in the Pin Description Table to Note 6<br>(2) Add Pin Description Note 6 Description<br>(3) Updated the system block diagram |
| 2/22/2021 | 1.2 | (1) Modify HXT-HSECLK<br>LXT-LSECLK<br>HIRC-HSICLK<br>LIRC-LSICLK<br>USB-USBD<br>(2)Modify the wrong name of PA14 pin in the pin definition<br>(3) Change STO:STA in Figure 15 to STA:STO |
| 8/9/2021 | 1.3 | (1) Will be in the clock tree "4-16 MHZ LSICLK OSC" correction for "4-16 MHZ HSECLK"<br>(2) Delete all details and names which are about APM32F103x4x6x8 |